MULTICHANNEL ANALYZER

Model 4100

Instruction Manual

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Section 1
INTRODUCTION

The Model 4100 Multichannel Analyzer is a data acquisition, display and output unit. It can perform two basic acquisition cycles:

1. PHA (Pulse Height Analysis) - number of occurrences of signal amplitude.

2. MCS (Multi-Channel Scaling) - number of occurrences as a function of time.

Although designed primarily for analyzing various aspects of nuclear physics, the Model 4100 may be used to analyze other parameters that may be expressed in terms of voltage or time.

An active filter pulse amplifier, SCA and 50 MHz Wilkinson type ADC are part of the standard analyzer. An optional High Voltage Supply (0 to 3000V) suitable for nuclear detectors can be included in the Omega 1.

Inputs are digitized and stored in the processor memory where they can be read out for display on the built-in CRT. The display consists of the data in analog form as well as the alpha-numeric display of important parameters such as channel contents, integrals, channel address, etc. The Compare and Strip functions are a standard feature. Both are Display features and do not affect memory contents. Compare provides an analog comparison of the halves of the memory contents. One half may be variably attenuated zero to 100%. Strip provides a means of subtracting a variable (zero to 100%) portion of one half of the memory from the other half. A 256 channel semiconductor memory is standard. 512 and 1024 channel memories are options. Each channel of the memory can store 999,999 counts. Stored data can be read out in analog form to XY or strip chart recorders. Options provide read out to teletype, printer, magnetic tape, and RS232C compatible devices such as modems, terminals and computers.

SPECIFICATIONS

2.1 GENERAL

2.1.1 DISPLAY FUNCTION

Data in memory is displayed in analog form on the built-in 5-inch CRT. Vertical displacement is proportional to count level and horizontal displacement is proportional to channel number. An alpha-numeric* read out of important parameters can be provided on the CRT.

2.1.2 COLLECT FUNCTION (Data Acquisition)

Pulse Height Analysis (PHA) - Number of occurrences as a function of amplitude. Bipolar pulse amplifier and Wilkinson type analog to digital converter (ADC) are included.

Multi-Channel Scaling (MCS) - Number of occurrences as a function of time.

2.1.3 INPUT/OUTPUT FUNCTION (I/O)

Data stored in memory can be read out in analog form to a plotter or to a digital* recorder. Digital information can be loaded into memory.*

2.1.4 MECHANICAL

SIZE	Table Top; 9-1/2 inches high (24 cm.), 17 in. wide (43 cm.), approximately 21-1/2 inches deep (55 cm.) (overall) Rack Mounting adapter available*
WEIGHT	Approximately 50 lbs. (22.5 kgs.)
POWER	105 to 125 VAC or 210 to 250 VAC (Switch Selectable) Internal Jumpers for 95 to 115 or 115 to 135 VAC (190 to 230 or 230 to 270 VAC) 50 to 65 Hz approximately 220 watts
OPERATING TEMPERATURE	0 to 45° C ambient with adequate air flow for fan at rear

2.2 MEMORY

NUMBER OF CHANNELS	256 Standard; 512 or 1024 optional
COUNT CAPACITY	10^6-1 per channel
TYPE	Semiconductor
CYCLE TIME	2.5 μs per digit
MEMORY CONTROL	Selects memory group to be addressed and digital range (overflow) of ADC. Selection is full or either half. In all further references to the memory only the selected group is affected.
RESET	In Display or Dynamic Collect Modes, data is cleared by pressing two toggle switches. Channel Zero can be reset in Display by pressing the Channel 0 Reset Switch.

*Optional

TRANSFER	In Display or Dynamic Collect Modes, data can be transferred to the selected half of the memory from the other half by raising both the transfer switches.
ARITHMETIC	Add, Subtract or Off
MEMORY TEST	Internal Switch adds (or subtracts) one count per sweep in each digit of the selected vertical range.

2.3 ANALOG SECTION

2.3.1 AMPLIFIER

TYPE	Bipolar with 1.5 μsec near - Gaussian pulse shaping; Bipolar pulse width 10 μsec; Optional plug-on boards available for changing the time constant.
INPUT	Positive or negative tail pulse; less than one μs rise time; Input impedance 300 ohms; Maximum input 6 volts; Front and real panel BNC connectors.
POLE-ZERO	Internal adjustment factory set for 50 μsec preamp fall time constant.
GAIN	10 to 1000
GAIN CONTROLS	Coarse: 4 position rotary - 30, 100, 300, 1000 Fine: 10 turn locking pot - 0.3 to 1.0
INTEGRAL NONLINEARITY	$< \pm$ 0.1% of full scale
DRIFT	Gain: less than $\pm$ 0.02% of full scale/^{o}C Zero: less than $\pm$ 0.01% of full scale/^{o}C
NOISE	$<$ 15 μv RMS referred to input at maximum gain with input terminated and using standard pulse shaping time constants.
OVERLOAD RECOVERY	Within 2% of baseline in 60 μsec from X750 overload
PREAMP POWER	$\pm$ 24V, $\pm$ 12V and ground on rear panel connector compatible with Canberra preamps. Current available from each supply is 50ma maximum except +12V from which 75ma is available.

2.3.2 SCA

INPUT	DC coupled to ADC Input; Range -0 to +11 volts
OUTPUT	Positive 4 volt logic pulse; approximately 0.5 μsec width; operates independently of ADC dead time; Rear panel BNC connector.
LOWER LEVEL (LLD)	10 turn locking pot; sets lower limit of SCA and ADC window; 0 to 110% of range.
UPPER LEVEL (ULD)	Single turn pot; sets upper limit of SCA and ADC window; 0 to 110% of range.

TIMING	Output pulse generated when input pulse falls through the LLD setting.
INTEGRAL NONLINEARITY	< ± 0.25% of full scale
DRIFT	< ± 2 millivolt/^{o}C
PULSE PAIR RESOLUTION	1 μsec minimum

2.4 ADC

SIGNAL INPUT	Switch selectable from internal or external amplifier; positive unipolar or bipolar pulses; 0 to +10 volt full scale range; Front and rear panel BNC connectors; Rise Time - greater than 250nsec less than 30 μsec (with longer rise time made acceptable on request); Pulse Width - greater than 1 μsec; Input impedance - 2.2K; Maximum input - +12 volt
GATE INPUT	Logic pulse or level; +3 to +10V; width greater than 250 μsec; front and rear panel BNC connectors.
METER	Percent of time ADC is busy
CONVERSION GAIN	4 position rotary; selects resolution of full scale input signal; selection of 1 part in 2048, 1024, 512 or 256.
ADC WINDOW	Set by SCA, LLD and ULD Controls
DIGITAL RANGE	Set by Memory Control Switch
ZERO INTERCEPT	22 turn screwdriver adjustment on front panel; Range approximately ± 5% of full scale Resolution less than 0.01% of full scale
DIGITAL OFFSET	Three toggle switches: 1024, 512 or 256 channel offsets (0 to 1792 in 256 channel increments)
LINEAR GATE	Peak detector circuitry closes gate
INTEGRAL NONLINEARITY	Less than ± 0.05% over top 98% of full scale range
DIFFERENTIAL NONLINEARITY	Less than ± 1% over top 98% of full scale range
DRIFT	Gain less than ± 0.02% of full scale/^{o}C Zero less than ± 0.02% of full scale/^{o}C Long Term less than ± 0.02% of full scale per 24 hours at constant temperature
CONVERSION CLOCK	50 MHz; crystal controlled; at 512 and 256 Conversion Gain the conversion clock is divided by a factor of 2 and 4 respectively

GATE	With no input connected conversion is enabled in either switch position (Anti or Coinc) Coincidence: Positive Pulse received during Linear Gate Time will allow conversion Anti: Positive Pulse received during Linear Gate Time will prevent conversion Internal jumpers to change gating for Early gating mode which requires gate level at time the LLD is crossed.

2.5 DETECTOR HIGH VOLTAGE POWER SUPPLY*

VOLTAGE	0 to 3000 volts
CURRENT	0 to 2 ma - Short circuit proof and self restoring
POLARITY	Positive or Negative; Internal switch controlled
POLARITY INDICATION	Front Panel LED lamps
RIPPLE AND NOISE	Less than 10 mv peak to peak
DRIFT	Temperature: less than ± 150 mv/^{o}C Long Term: less than ± 600 mv/8 hrs.
REGULATION	Line and load less than ± 300 mv
CONTROL	5 position rotary and 10 turn locking pot; Output is sum of the two control settings; Rotary - 0, 500, 1000, 1500, 2000 Pot - 0 to 1000V
CALIBRATION ACCURACY AND LINEARITY	Within ± 10 volts of Control reading
RESETABILITY	Within ± 0.5 volts

2.6 DISPLAY FUNCTIONS

2.6.1 CRT DISPLAY

SIZE	4 1/2" (11.4 cm) rectangular viewing area (3.4 x 2.4 in., or 86 x 61 mm)
CRT controls	Intensity; Focus

2.6.2 DATA DISPLAY

VERTICAL RANGE	Linear: 99: 999: 9,999: 99,999: 999,999 Resolution: 1/1000
VERTICAL GAIN	X1 to X10 gain, continuously variable; Calibrate Position X1 indicated by pot detent.
VERTICAL BIAS	10 turn control
HORIZONTAL RANGE	Full or half memory Resolution: 1 channel

*Optional

HORIZONTAL GAIN	X1 to X10 gain; continuously variable
HORIZONTAL POSITION	4 turn control
SCAN RATE	50,000 Channels/Sec maximum
CHANNEL IDENTIFICATION*	Cursors: brightened vertical markers Region of Interest: brightened in Intensify mode
ALPHA-NUMERIC READOUT*	Characters displayed on CRT; Start and Stop addresses; Data Word - contents of Stop Cursor, Integral or contents of channel zero: data word identified by C (Cursor), T (Time in Live PHA Collect), F (Full Memory Integral) or R (Region of Interest Integral).

2.6.3 SWITCH FUNCTIONS

SCAN LEVER CONTROL*	Controls position of Cursors; Cursor toggle selects movement of Start or Stop or both Cursors.
INTENSIFY*	Causes Region of Interest to be brightened during Display or Dynamic PHA Collect and transferred during Readout. The left Cursor designates the starting address of the ROI; the right Cursor designates the stop address.
INTEGRATE*	Integrates the ROI (Intensify ON) or full memory less ch 0. When enabled, the Integral will be displayed on the CRT and readout to the selected digital recorder.
DYNAMIC	In PHA Collect allows normal static Display functions to operate. Memory is timeshared by ADC and display logic. In Dynamic the ADC dead time is increased by an average of approximately 12 μsec.
COMPARE	Allows user to overlap halves of the memory and to compare on the CRT a percentage of the reference half with the half selected by the Memory Control. Memory data is not changed.
STRIP	Allows user to subtract on the CRT a percentage of the reference half from the half selected by the Memory Control. Memory data is not changed.
PERCENT POT.	10 turn locking pot calibrated 0 to 100% used for Compare and Strip functions.

2.7 COLLECT FUNCTIONS

2.7.1 PULSE HEIGHT ANALYSIS (PHA)

PRESET TIME

CORRECTION:	Live timer; 1 MHz crystal controlled clock is gated with ADC dead time. The pulse train is gated off when ADD-SUB switch is in the OFF position.
STORAGE:	Gated Pulse train pre-scaled to one second and added to contents of Channel Zero (Time Channel).

PRESET:	Two digit thumbwheels to select limit; N X 10^M where N is 1 to 9 and M is 0 to 5 (1 to 9 x 10^5 sec - 250 hours); With N = 0 the internal preset is disabled.
COLLECT STOP INPUT	Logic pulse input to rear panel BNC.
LIVE DISPLAY	Display point generated by ADC storage cycle. Numeric readout of Channel Zero.
DYNAMIC	Static Display of data and numeric readout; Memory is timeshared by ADC and display logic.

2.7.2 MULTICHANNEL SCALING (MCS)

MCSS	Single Sweep
MCSR	Recurring Sweeps
COUNT INPUT	Positive logic pulse; 100nsec pulse pair resolution minimum (10MHz); pulse width > 55nsec.
DWELL TIME PER CHANNEL	Selected by Preset Time switches; Dwell Time equals N X 10 M micro-seconds when N is 1 to 9 and M is 1 to 5 (100 μsec to 0.9 sec); with N=0 or M=0 or 1, the internal advance is disabled.
CHANNEL DEAD TIME	24 μsec
SWEEP TRIGGER	Internal or External Positive Logic pulse input. Pulse width of External Trigger must be greater than 1 μs.
SWEEP OUT	Positive Logic Pulse at Start of Sweep
EXTERNAL ADVANCE	Positive Logic Pulse input. Minimum Dwell Time 100 μsec. Minimum pulse width 1 μs. Maximum pulse width is 20 μs.
COLLECT STOP INPUT	External Counter can end Collect at completion of Preset Sweep by generating a logic pulse to the Collect Stop input. Pulse can come at any time during the final sweep.

2.8 READOUT FUNCTION

I/O (INPUT/OUTPUT)*	Data and integral information can be read out; data can be read in.
NORMAL	Data in the selected memory group will be transferred.
INTENSIFIED*	Data in Channel Zero and in the Region of Interest will be transferred.

*Optional

DIGITAL I/O

Tagword: Analyzer can be used with Canberra data modules. The data words in the modules precede the Analyzer data.

Integrate* The integral of data in the region of interest or memory group and the address of the Start and Stop channel will be read out.

Format: A format specification for each I/O device is given in the Appendices.

2.8.1 I/O CYCLE

MANUAL — Collect and I/O started manually.

SINGLE — I/O starts at end of Collect; Display mode starts after I/O is finished.

RECYCLE — After Collect ends, data is readout, memory data is reset, and Collect is re-started.

ANALOG RECORDER OUTPUT — Data can be recorded in linear form via a line or point plotting X-Y or T-Y recorder. Gain and Position effected by display controls.

X & Y: 0 to +5V full scale

Output Impedance: approximately 1K

Nonlinearity: < ± 0.1% of full scale

Resolution: X 1/Memory Group Size
Y 1/1000

Internal Timing: 1.5 to 10 Channel/Sec (adjustable by resistor change)

External Timing: For Point Plotters determined by Plot Complete signal up to 5000 Channels/Sec. Minimum rate ≈ 1.5 Channels/Sec.

DAISY CHAIN* — Plug-in option to allow the analyzer to be used with Canberra data module or scanner for control or data readout. Includes two 8-foot cables (Requires Basic Readout Option).

TTY* — Characters are typed in page form and can be punched in ASCII code on paper tape. Start. Stop, and every 100th data channel addresses are printed for identification. Format compatible with 8100 for identification. Format compatible with 8100 output. Requires Basic Readout option. With TTY interface installed Daisy Chain Scanner cannot be used for readout, but data modules (scalers, timers, etc.) in daisy chain can be read out through MCA to TTY.

2.9 REAR PANEL CONNECTORS

2.9.1 BNC SIGNALS

Signal characteristics - Except where noted:

	Inputs	Outputs
Logic 1:	+3 to +10 V.	+5V; 1K impedance
Logic 0:	+0.3V to -5V.	0.4V max; 10 ma
Impedance:	approximately 10K	-
Pulse Width:	500 μsec minimum	-

Amp Input (J101) - Analog input to amplifier	
INPUT	Positive or negative tail pulse
MAXIMUM VOLTS	6
INPUT IMPEDANCE	300 ohms
RISE TIME	$< 1\ \mu s$
FALL TIME CONSTANT	Internal pole zero factory set for 50 μsec
ADC Input (J102) - Analog Input Converted to Digital number for PHA	
RANGE	0 to 10 volts full scale +12 volts maximum
RISE TIME	$>$ 250nsec $<$ 30μsec
PULSE WIDTH	$>$ 1 μsec
IMPEDANCE	2.2K
GATE INPUT (J103)	Logic Input for Coincidence or Anti-Coincidence gating of ADC input
SCA OUTPUT (J104)	Logic pulse output generated when input to ADC falls within SCA window.
PULSE WIDTH	$\approx$ 0.5 μsec.
OUTPUT IMPEDANCE	$<$ 10 ohms
MCS COUNT INPUT (J105)	Logic Pulse Train counted during Multi-scale Dwell Time
PULSE WIDTH	55nsec minimum
PULSE PAIR RESOLUTION	100nsec minimum
LOGIC ZERO	-0.5 to +0.4V
MCS TRIGGER INPUT (J106)	Logic Pulse to trigger start of Multi-scale Sweep. With no input connected, the sweep will trigger automatically. Pulse width greater than 1 μs.
MCS ADVANCE INPUT (J107)	Logic pulse to signal end of current Dwell time; Internal Dwell Timer is disabled by setting Preset Time and switches to N=0 or M=0 or 1.
MINIMUM DWELL TIME	100 μsec
PULSE WIDTH	1 μsec minimum and 20 μsec maximum
MCS SWEEP OUT (J108)	Logic Pulse to signal start of each Multi-scale Sweep.
PULSE WIDTH	$\approx$ 20 μsec
COLLECT STOP INPUT (J109)	Logic Pulse to end Collect Mode; in PHA Collect will end after current cycle ends; in MCS, Collect ends after current sweep is completed.

2.9.2 OTHER REAR PANEL CONNECTORS

PREAMP POWER (J114)	9 pin Amphenol 17-10090 compatible with Canberra Preamps ($\pm$ 12 V, $\pm$ 24V and ground).
PLOTTER (J113)	25 pin Amphenol 17-10250. X and Y analog signals, Plot Enable level, Completed Plot Command input and Seek output.

HIGH VOLTAGE OUT* (J116)	MHV Connector; 0 to 3000 volt for Detector; Voltage set by front panel controls; Polarity set by internal control. SHV Connector with later units
DAISY CHAIN CONTROL OUT* (J120)	15 pin Amphenol 17-20150
DAISY CHAIN CONTROL IN* (J121)	15 pin Amphenol 17-10150; provides connection between MCA and Canberra Daisy Chain for readout through Scanner (1488, etc.), or for readout of Modules through the Analyzer's Digital Interface.
TTY OUT* (J117)	9 pin Amphenol 17-10090; provides connection to TTY Printer Punch; 20 ma current loop: Motor Control relay drive (+24V) provided for modified TTY.
EIA OUT* (J118)	25 pin Amphenol 17-10250; Provides connection to Data Set or EIA compatible Terminal or Computer.

2.10 4100 SYSTEM CONFIGURATION

2.10.1 STANDARD

Pulse Amp
SCA
50 MHz ADC with 2048 channel resolution
256 channel semiconductor memory
10^6-1 Count capacity
CRT
Display Comparison and Spectrum Stripping
Plotter Read Out
Instruction Manual

2.10.2 OPTIONS

Data Handling

02 Integrator Cursor-Character Generator (needed for digital and selective readout, cursor and character generation on CRT).

Read Out	
04	Basic Read Out (requires 02)
04B	HP 7004B Point Plotter Cable
04C	General X-Y Plotter Cable
04Z	Basic Read Out and Integrator (provides Read Out and Integration of Full memory group only)
**05	TTY Interface (requires 04/04Z and cable)
S1488	TTY modification kit and cable
C1488	Cable to Standard TTY. Spade Lugs at TTY end.
**05A	TTY Interface EIA Compatible Asynchronous Line Interface with cable for EIA output - 04/04Z and cable to TTY.
**05B	T1733 Interface, EIA RS232 Levels (requires 04/04Z)
06	NIM Daisy Chain Interface with two 8-foot cables (requires 04/04Z)
**07A	MDS Printer Interface and Cable (require 04/04Z)
**07B	HP 5055A or HP 5050B Printer Interface and Cable (requires 04/04Z, Specify Printer)
**07C	Newport 810FP Printer Interface and Cable (requires 04/04Z)

*Optional

Memory	
08	512 channel semi-conductor memory
09	1024 channel semi-conductor memory
Analog	
03	Detector High Voltage Power Supply (0 to 3000 volts)
10A	Amplifier shaping - Time Constant 3 μs
10B	Amplifier shaping - Time Constant 6 μs
Miscellaneous	
11	19" Rack Adaptor
12	Service Kit includes schematics, extender boards, lamps, spare fuses, knob tools, pot adjuster and service feet.
Read In/Read Out	(Available on later units)
**15	TTY Interface (requires 04/04Z and cable)
**15A	TTY Interface/EIA compatible Asynchronous Line Interface with cable for EIA output (requires 04/04Z and cable to TTY.)
**15B (S)	TI733 Interface EIA RS232 Levels (requires 04/04Z). S version transfers at 1200 Baud instead of 300.
**15C	PTR306 (Centronics) Interface EIA RS232 Levels (requires 04/04Z). Read Out only.
**15T	TTY Interface/Techtran 8410 Cassette Interface (requires 04/04Z and cable to TTY).
**15L	Decwriter Interface with Cable (20mA current loop).

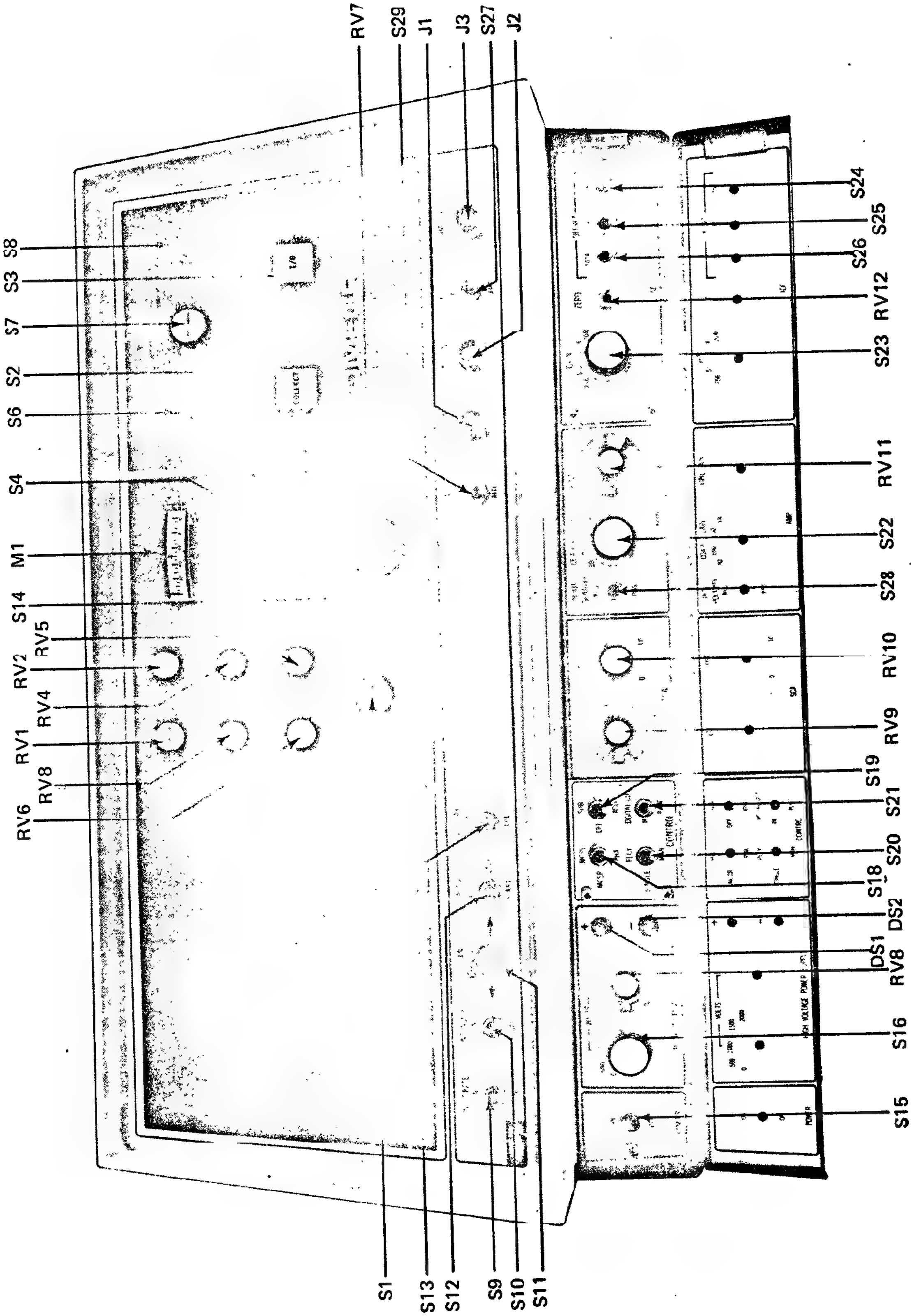
**Total of one per Chassis

Section 3
CONTROLS, CONNECTORS, AND METER

3.1 FRONT PANEL

3.1.1 UPPER FRONT PANEL

INTENSITY (R1)	Controls brilliance of CRT
FOCUS (R2)	Adjusts clarity of the display
HORIZ GAIN (R8)	Adjusts horizontal deflection sensitivity of data display. Does not effect numeric display. Gain range is from 1 to 10.
HORIZ POS (R4)	Used with HORIZ GAIN to position any portion of the data display on the CRT. Four turn control.
VERT GAIN (R6)	Adjusts vertical deflection sensitivity of data displayed; does not effect numeric display: range is from 1 to 10; calibrated position (X1) is marked and has detent.
VERT BIAS (R5)	For normal display and the Strip function. adjusts vertical position of data displayed; does not effect numeric display. When comparing memory halves, it positions the reference segment. Ten turn control.
VERT RANGE (S1)	Settings 10^2-10^6 establish vertical range of display.
ADC DEAD TIME % (M1)	Indicates the percentage of time the ADC is not able to accept pulses.
PRESET TIME (S4A, B)	Two digit thumbwheel switch used to select PHA preset time or MCS dwell time.
STRIP-COMPARE-OFF (S14)	Used to select Compare or Strip mode of operation in Display or Dynamic Collect (PHA). No function during Readout or with Memory Control in full.
% (R7)	10 Turn Control - The % control determines the factor by which the reference data is attenuated. The Memory Control switch selects the non-reference spectrum (half). The other non-selected half is the reference spectrum. During Compare, the attenuated reference spectrum is compared to the non-reference spectrum. During Strip the attenuated reference spectrum is subtracted from the non-reference spectrum.


RV7
S29
J1
J3
S27
J2
S8
S3
S7
S2
S6
S4
M1
S14
RV5
RV2
RV4
RV1
RV8
RV6
S24
S25
S26
RV12
S23
RV11
S22
S28
RV10
RV9
S19
S21
S20
S18
DS2
DS1
RV8
S16
S15
S1
S13
S12
S9
S10
S11

MEMORY CONTROL (S7)	Selects memory group to be addressed during all modes of operation. Full enables use of entire memory and disables Compare and Strip. 1/2 enables use of first half of memory. 2/2 enables use of the second half of memory. In PHA the size of the memory group selected will determine the digital overflow of the ADC address register. A/2 (Non-standard) allows operation with 8220 Mixer Rooter.
TRANSFER (S6, S8)	In Display or Dynamic Collect setting both switches up causes the transfer of data to the selected memory half from the half not selected Transfer is non-functional when Full memory is selected.
RESET (S6, S8)	In Display or Dynamic Collect setting both switches down causes the entire memory group to be reset to zeros. In Display, setting the CH0 Switch (S6) down will cause channel zero be be reset to zero.
COLLECT (S2)	Manual control and indication of activation of Collect function.
READ OUT (S3) (I/O)	Manual control and indication of activation of Read Out function. I/O nomenclature indicates capability of Read In also.
INTEGRATE (S9)*	Selects Integrate mode of operation during Display, Dynamic Collect, or Read Out. During Display or Dynamic Collect the full memory group selected or the region-of-interest integral will be displayed on the CRT. During Read Out, the integral and the start and stop addresses over which the integral is taken are recorded.
INTENSIFY (S10) *	During Display or Dynamic Collect the data points, on the CRT, between the start and stop cursors become a region-of-interest (includes start cursor but not stop cursor). The display locations in the ROI are brighter than in normal display, and the integral displayed will be that of the ROI. It causes Read Out to be selective, allowing only read out of the ROI data and ROI data Integral.
SCAN (S11)*	Controls motion of Cursor(s). Controls direction and rate of cursor movement. Quick, momentary, switch deflection causes single channel increment or decrement. Holding the switch in either direction causes the cursor(s) to move in that direction at a rate determined by the time the switch is held ON. Maximum rate is approximately 300 steps per second.

*Optional

CURSORS (S12)*	The control which selects which cursor may be moved by the scan switch. Both indicates the Start and Stop cursors may be moved together. Stop indicates only the Stop or cursor-on-the-right may be moved. Start indicates only the Start or cursor-on-the-left may be moved.
DISPLAY (S13)	Used during PHA to enable the Dynamic Display mode. During Collect, Display and PHA cycles are time-shared to create a normal or static display. Dynamic increases the average dead time.
GATE (S29)	Used to select either Coincidence or Anti-Coincidence modes.
GATE IN (J1)	Positive Logic Pulse, +3 to +10V amplitude, width > 250 ns. With no input connected to GATE IN analysis will be enabled in either position of the switch (Anti or Coinc). If a Coincidence signal is connected, a positive pulse during the Linear Gate time is necessary to enable conversion; this is called "late" coincidence. In the Anti position, a positive pulse during the Linear Gate time is necessary to prevent the conversion. Internal jumpers are provided to change gating for "early" gate mode.
ADC IN (J2)	Positive signal directly coupled to ADC and SCA inputs if selected by Input switch.
INPUT (S27)	Selects the source of signals for the ADC and SCA. When ADC is selected, the source is from an external amplifier. When AMP is selected the internal amplifier is the source of signal.
AMP IN (J3)	Input connector for the internal amplifier, from a preamplifier.

3.1.2 LOWER FRONT PANEL (behind door)

POWER (S15)	Controls power (line voltage) to analyzer.
HIGH VOLTAGE POWER SUPPLY CONTROLS *	Used to control output voltage of the detector bias supply. The coarse output switch has 5 settings in increasing 500 volt increments. The fine output control is variable from zero to 1000 volts. The output voltage on the rear panel (J116) is the sum of the two settings. The + and - indicators indicate the polarity of the output voltage.
MCSS-MCSR-PHA (S18)	Control selector for Collect function. PHA - Pulse Height Analysis MCSR - Multi-channel scaling, recurring sweeps MCSS - Multi-channel scaling, single sweep

*Optional

RECY-SINGLE-MAN (S20)	Control selector for Collect-Read Out sequencing. RECY - When Collect ends, data is read out, the memory group reset, and Collect is restarted. SINGLE - When Collect ends, data is read out, the memory is not reset. The system is then set into Display. MAN - Collect and Read Out functions are started manually.
SUB-OFF-ADD (S19)	Switch selects modification of arithmetic data during Collect or Display Test memory cycles. In OFF the memory location data is not altered.
DIGITAL-PLOT DIGITAL OUT - IN - PLOT (S21)	Provides selection of peripheral device. Analog output to plotter is determined by the display position and gain controls. Digital Output/Input is optional.
SCA-LLD (R9)	10-turn locking pot. Used to select lower limit of the SCA and ADC windows. Range is 0 to +11V.
SCA-ULD (R10)	Single turn pot. Used to select upper limit of the SCA and ADC windows. Range is 0 to +11V.
INPUT POLARITY (S28)	Used to provide a negative or positive choice for the input signal to the Amplifier.
AMP COARSE GAIN (S22)	4 position switch selects Amplifier gain. Settings are 30, 100, 300 and 1000.
AMP FINE GAIN (R11)	10 turn locking pot to adjust gain by factor from 0.3 to 1.0.
ADC GAIN (S23)	4 position rotary selects the full scale resolution of a 0 to +10 volt input signal. Resolution is one part in 2048, 1024, 512 or 256.
ADC ZERO (R12)	Multi-turn screwdriver adjustment of analog zero. Control is factory-set to put 0 volts (energy) into channel zero with a Conversion Gain of 1024, 512 and 256.
ADC OFFSET (S26, S25, S24)	Three toggle switches provide digital offsets of the ADC output (to the memory). The offsets are 256, 512, and 1024 (0 to 1792).

3.2 REAR PANEL

3.2.1 STANDARD CONNECTORS

230/115 Line Voltage selector switch S101 should be positioned such that the marking of the voltage used is seen through the hole in the panel.

FUSES - F101, F102	Line Fuses for 115 volt operation are 3 amp Slow Blow; for 230 volt operation are 1 1/2 amp Slow Blow.
AMP INPUT (J101)	Input connector to the internal amplifier. Wired in parallel with J3 on front panel.
ADC INPUT (J102)	Positive signal directly coupled to ADC and SCA inputs if selected by Input switch. Wired in parallel with J2 on front panel.
GATE INPUT (J103)	Positive logic pulse used to gate ADC. Wired in parallel with J1 on front panel.
SCA OUT (J104)	Positive logic pulse from SCA. Indicates the input pulse amplitude has exceeded the LLD setting but is less than the ULD setting.
COUNT IN (J105)	Positive logic pulse input to MCS counter during MCSR or MCSS Collect mode.
TRIG IN (J106)	Positive logic pulse starts sweep during MCSR or MCSS Collect. If no input is connected auto triggering results.
ADV IN (J107)	Positive logic pulse causes dwell time to end during MCSR or MCSS Collect mode. Preset Time selector must be 00 for proper operation.
SWEEP OUT (J108)	Positive logic pulse out at the start of each sweep in MCSR or MCSS Collect.
COLLECT STOP (J109)	Positive logic pulse input ends Collect function.
PLOTTER (J113)	Connects signals to Plotter (25 pin)
PREAMP POWER (J114)	Connector to supply power to Canberra Preamps (9 pin).

3.2.2 OPTIONAL CONNECTORS

The following connectors are installed only as options. Additional covered cutouts have been provided in the rear panel for future options.

AUXILIARY (J115)	Used for special applications.
HIGH VOLTAGE OUT (J116)	Output from Detector Bias Supply. Adjustable by front panel control from zero to 3000V. Polarity selectable by internal switch.

TTY (J117)	Output connections for a 20 ma. current loop teletype (9 pin).
EIA (J118)	Output connector to a Data Terminal or Data Set compatible with EIA (RS232) (25 pins)
EIA (J119)	Same as J118, but uses Dataphone type of adapter.
CONTROL IN (J120)	Daisy chain connector for use with Canberra NIM (15 pin).
CONTROL OUT (J121)	Daisy chain connector for use with Canberra NIM (15 pin).
OUTPUT SELECTOR (S102)	Used with 05A, 15A, and 15T options. Provides selection of Teletype or EIA Output. A third position allows remote selection of the device.

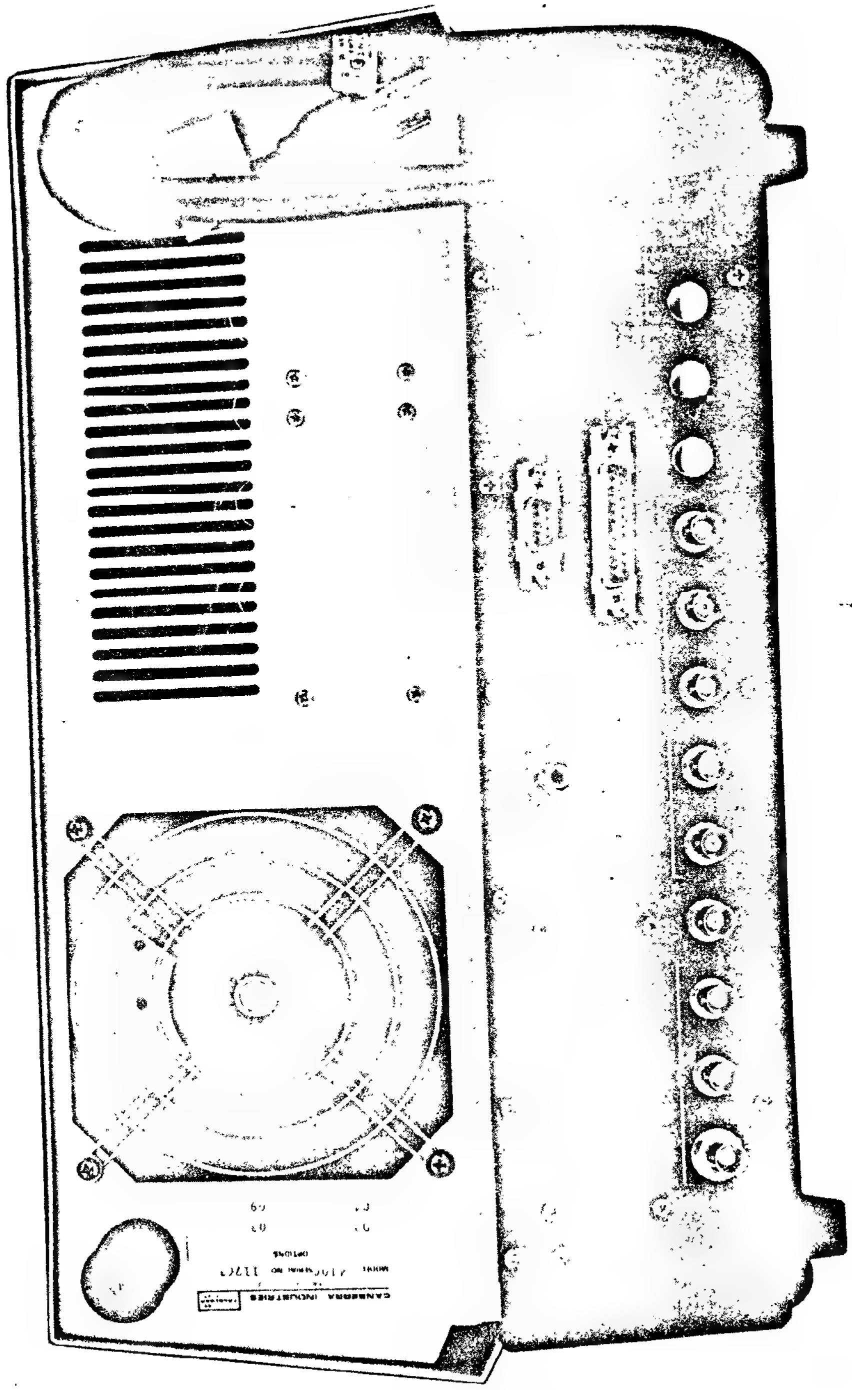


Figure 3-2. Model 4100, Rear Panel

Section 4
PREPARATION FOR USE

4.1 UNPACKING

The Omega 1 is shipped in a specially-designed box which protects the instrument against damage. When removing it from the shipping box, perform a visual inspection. If any damage has occurred in shipment, notify the carrier and your local Canberra sales office.

4.2 INSTALLATION

4.2.1 GENERAL

The AC line selector on the rear panel should be checked for the proper position.

The unit is meant to be placed on a table. An adapter is available for rack mounting.

The unit should be positioned so that the fan at the rear will have adequate air flow.

THERMAL CUT-OUT

If the internal temperature of the Analyzer rises above a safe level, a thermal cut-out will turn off the power.

4.2.2 PRELIMINARY CHECKOUT

The purpose of this section is to perform a few simple tests to determine if the analyzer's main functions are operating.

1. Connect to AC power line.
2. Open door below handle.
3. Turn on power.
4. Neither the Collect or Readout lamps should be on; the fan should come up to speed and, after ≈ 30 seconds, a display should be visible.
5. If the Integrator-Cursor-Character Generator (option 02) is installed, the display should include 3 sets of numbers below the lined graticule area.
6. In the Control section (below the handle), set the toggles to PHA, ADD, Man and Plot.
7. Set the Preset Time thumbwheels to *21* (20 seconds).
8. Set the Vertical Range to 10^2.
9. Reset Memory by pressing both reset switches down at the same time.
10. Select Live Display.
11. Start Collect by pressing the Collect button.
12. The Collect lamp should come on.

13. It should be possible to see channel zero incrementing ≈ once per second. With the 02 option, the numeric contents of channel zero should be given by the character generator. The time word is identified by the T suffix.

14. After 20 seconds, the Collect function should end and the normal Display be resumed.

15. Disable Intensify. This function only operates with the 02 option.

16. Start Readout by pressing the Readout button.

17. The Readout lamp should come on.

18. The CRT should show a slow advance (< 1 per second) through the memory. Increase the Scope Intensity if not visible.

19. End Readout by pressing the Readout button and holding it in for about a second until the lamp goes out.

20. The Display function should be resumed.

These checks will indicate that the analyzer is functioning. Refer to further sections and the Appendix for specific operating instructions.

4.2.3 RACK MOUNTING

The rack mounting adapter available from Canberra (option 11) fits into a standard 30-inch deep by 19-inch wide rack. When mounted, the analyzer and frame uses 10 1/2 inches of vertical dimension.

To install:

1. Remove feet and tilt stand from bottom cover of 4100.

2. Place 4100 into adapter. Line up the cut-outs for air flow and attachment holes (feet). This step can be done with analyzer in rack if area below analyzer is accessible.

3. Secure the analyzer to adapter by screws through bottom of shelf into the holes on the analyzer previously used for the feet.

4. If not previously done, mount adapter and analyzer into rack using mounting bolts to front and rear rails.

5. Place frame over top of analyzer to fill in the front panel area and secure frame to rack.

4.2.4 INSTALLATION WITH PERIPHERAL EQUIPMENT

Connect the cable(s) to the appropriate cable connector. Refer to Section 5, Appendix and peripheral unit manual for details.

4.2.5 TOP COVER REMOVAL AND INSTALLATION

1. Remove the six (6) side screws.
2. Pull cover toward rear until the rear PEM nuts on cover touch the back panel.
3. Bow the lower rear corners of the top cover, lift and pull the cover toward the rear until the PEM nuts clear the rear panel.
4. Lift the cover straight up.
5. Reverse the procedure for installing the top cover.

4.2.6 INSTALLATION OF OPTIONS

... the Locator drawing

Section 5
OPERATION

5.1 GENERAL

The analyzer has three basic states. These are:

Collect
Read Out
Display

Both Collect and Read Out are indicated by their respective lighted switches. Display does not have an indicator, but if the Read Out and Collect lights are not on, the analyzer is in the Display state. When the Analyzer is first turned on, automatic reset circuitry puts it into Display with all other functions off. A similar, manual reset is performed by pressing the Collect and Read Out buttons simultaneously. To activate a function, the respective pushbutton switch is depressed. To disengage it, it is pushed again. The light in each switch is used to acknowledge the actuation of the state. The analyzer can not be in Collect and Read Out simultaneously. To disengage Read Out, it is necessary to hold Read Out depressed until the word being transferred is completed. The semiconductor memory is volatile. Turning the power OFF causes the memory data to be lost.

Without the 02 option, the standard Model 4100 has no Alpha-numeric character display, and the following switches will have no function:

INTEGRATE
INTENSIFY
SCAN
CURSORS

With the 04Z option installed, the Integrate switch will function in Read Out to give a full memory integral (less channel zero).

5.2 DISPLAY

5.2.1 INTRODUCTION

The Display state is used to indicate to the user the data in the memory without changing this data. The section of the memory to be displayed is indicated by the Memory Control switch. The selections are Full, 1/2 or 2/2 and provide display respectively of full, first half or second half of the memory. In further references to the memory, only the selected group will be affected. A standard analyzer contains 256 channels. 512 and 1024 channel memories are available as options. The memory section is normally displayed across the full width of the CRT. Horizontal gain and position controls have been provided to allow closer inspection of any part of the display. A fourth position, A/2, allows (with proper modification) operation with a Mixer Router.

The horizontal gain range is from 1 to 10. Each channel in the memory contains a maximum of 999,999 counts. The Vertical Range switch selects the deflection factor on the CRT. This can be varied by a factor of from 1 to 10 with the Vertical Gain pot. The Vertical Bias or position control is also convenient to use in changing the dynamic range of the display. Adjusting the VERT BIAS and VERT GAIN pots allows one to amplify a small peak riding on a high background. The location of the optional Start and Stop Cursors is indicated by two markers on the display of the memory data.

Appearing on the CRT, along with the analog representation of the data in the memory, are several character words formed by a character generator.* The words seen are the Start and Stop Cursor addresses, the memory contents at the Stop Cursor address, the integral of the area defined by the Start and Stop Cursors (not including the Stop Cursor), the full integral of the memory section (not including channel zero), and the contents of channel zero (Time). The specific words displayed at a given time are determined by the various front panel switch settings. Leading zeroes are suppressed.

5.2.2 DYNAMIC

In PHA Collect, the normal display (LIVE) is as the data is being stored in the memory. It is possible to have a display which sequentially sweeps through the memory presenting a bright flicker-free display. This is the Dynamic function. While in Dynamic the normal display logic time shares the memory with the ADC. It does add a small amount of additional dead time to the ADC (12 μs average). It is most valuable when looking at low count rate experiments. While in Dynamic, it is possible to reset the memory by depressing both of the Memory Control Reset switches. It is not recommended that Dynamic be used when an experimenter is striving for the highest resolution from the system because the Dynamic cycling causes some noise to be introduced into the ADC and amplifier. The switch, DISPLAY, may be set to LIVE or DYNAMIC at any time.

5.2.3 CURSORS*

The Cursors are pointers on the display. They are vertical markers riding on the data points. Giving them the names Start Cursor and Stop Cursor help indicate that they define a region, or band of channels. They are displayed during the Display and Dynamic-PHA-Collect states and can only be positioned such that the Stop Cursor location is equal to or greater than the Start Cursor location. The CURSORS switch selects which, or both, Cursor(s) will be moved. The SCAN switch determines the direction and enables movement. The rate of movement is proportional to the time that the SCAN lever is depressed, making it easy to make small or large changes. While the cursors are displayed, the character generator also places their addresses on the lower portion of the CRT display; the Start Cursor on the lower left, the Stop Cursor on the lower right.

5.2.4 INTENSIFY**

Intensify is an important function during Display, Dynamic-PHA-Collect, or Read Out. When ON, the region-of-interest (ROI) between the Start and Stop Cursors will be intensified more than the rest of the channels, creating a more easily seen band in the spectrum. The Start cursor channel is the first channel and the Stop cursor channel is the address of the channel following the last channel of the ROI. During Read Out, if Intensify is ON, only the data in the ROI will be transferred; otherwise, the full memory section will be transferred. Also, when Intensify and Integrate are ON, the integral will be that of the ROI. Full Integration takes place when Integrate is ON and Intensify is OFF.

5.2.5 INTEGRATE**

The Integrate function sums the contents of a particular area of the memory. In Display and Dynamic-PHA-Collect the integral can be seen on the CRT. The integral is updated approximately every four seconds. In Display, the area integrated is the following:

a. With Intensify OFF, it is the Memory group selected not including channel zero.

b. With Intensify ON, the integral is of the region-of-interest and may include channel zero. If the Start and Stop cursors are equal, the integral is blanked.

The integral can also be read out to the Teletype Printer. The integrals recorded are similar to display.

*Part of Integrator-Cursor Option

5.2.6 RESET AND TRANSFER

The Memory Reset and Transfer functions are activated by the same two momentary toggle switches. In Dynamic-PHA-Collect or Display, pushing both toggles down will clear the entire memory group selected by the Memory Control. Pressing the switch marked CHO down in Display will cause only the data in Channel Zero of the selected group to be reset. The Transfer function is enabled by engaging both toggles up. It causes data in the corresponding channels in the other half of the memory to be transferred to the memory segment selected by the Memory Control; the data in the other will not be changed.

Data is transferred in Display or Dynamic-PHA-Collect as follows:

Memory Control	Transferred From	To
FULL	NO TRANSFER	
1/2	2/2	1/2
2/2	1/2	2/2

5.2.7 COMPARE

The Compare feature overlaps halves of the Memory and attenuates the "reference half" a controllable amount. It enables one to determine quantitatively the ratio of one peak to another peak. It operates in Display or Dynamic-PHA-Collect with the Memory Control in either of the halves positions. The Vertical Range must be set such that both the data and reference peaks appear with no "fold over"; i.e., the maximum memory data is less than the Vertical Range. The Vertical Gain should be adjusted for maximum resolution. The reference peak must be larger than the peak to which it is being compared. If the reference peak is smaller, the Memory Control must be changed so that the reference and data roles will be reversed. When the STRIP-COMPARE-OFF switch is set to COMPARE and Memory Control is not FULL, Compare is enabled. The comparison factor (attenuation) is determined by the % control. A setting of full clockwise (100%) represents a factor of 1. The control is direct reading in comparison factor from 0.00 to 1.00 (zero to 100%). The Vertical Bias control positions only the reference spectrum and should be set to have the baseline of the two spectra overlap. An important point to realize is that the data in the memory will not be changed by using the Compare function; only the display of data is affected. If the Integral function is enabled, the integral displayed by the character generator is of the selected region in the data group of the memory.

5.2.8 STRIP

The Strip feature provides a means of attaining visual spectrum stripping (memory data is not altered). The resultant spectrum is A-%xB, where A is the Data spectrum, B the Reference spectrum, and % the multiplier factor (% control setting). Set-up is carried out by first setting Compare and obtaining the correct settings for Vertical Range and Vertical Gain. The peak amplitudes in the Reference spectrum should be matched to those that are to be stripped in the Data Spectrum. The % control provides the attenuation factor. The analyzer is next set into Strip and the resultant of the subtraction is observed. The Strip information is in analog form and is not available for Read Out.

5.3 COLLECT

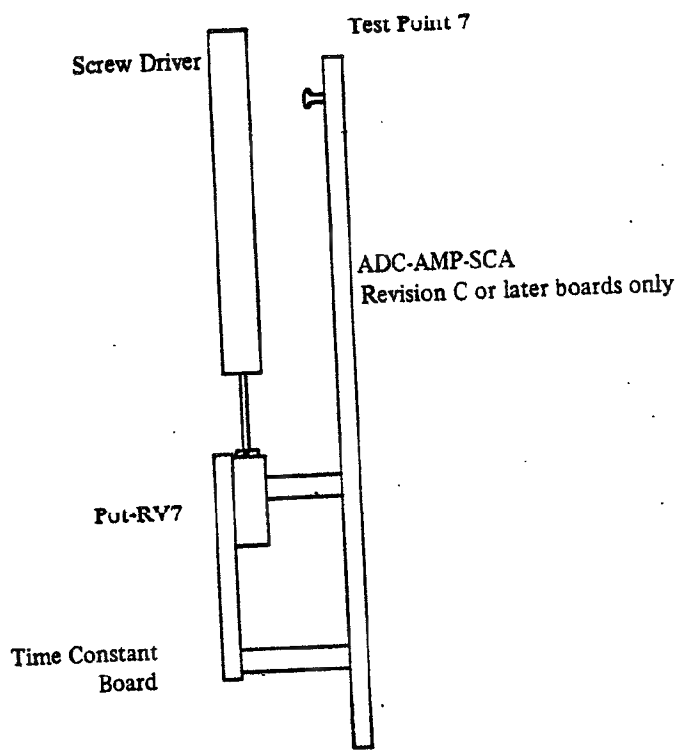
During Collect, raw data is digitized and stored in the memory. Several Collect functions will be described.

5.3.1 PHA

During PHA, pulses from nuclear detectors are sorted according to their amplitude into the memory. Live or Dynamic Display is selectable. Live display is usually preferable when setting up the experiment because the effects of changing gain, SCA window, or base line can be seen immediately.

5.3.1.1 AMPLIFIER

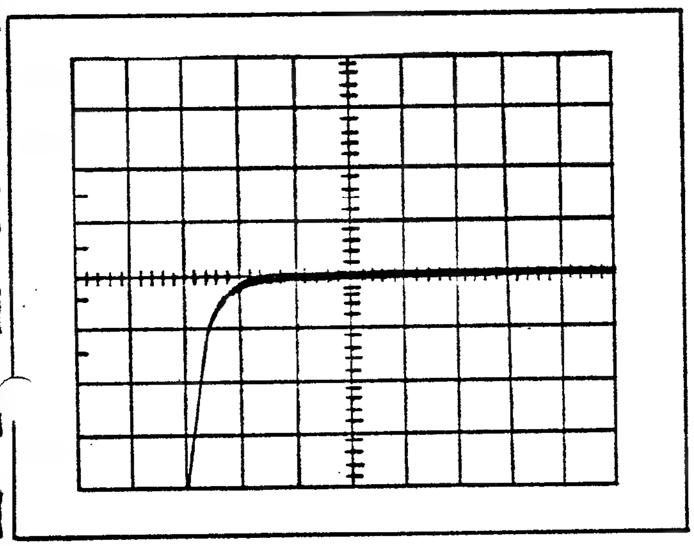
The internal amplifier accepts negative or positive pulses from a preamp and presents a bipolar 1.5 microsecond Gaussian-shaped pulse to the ADC. Optional plug-on boards are available to change the time constant. The amplifier is factory-set for a 50 microsecond fall time constant on its input (Pole-Zero setting). The bipolar amplifier is fairly tolerant of different fall time constants at low to medium count rates but at count rates above 5 KHz, the resolution of a Ge(Li) detector would be affected by an improper setting. It should be adjusted when changing pre-amps. To gain access to the adjustment pot it is necessary to remove the top cover. The pot is mounted on the Amplifiers Time Constant board and requires the use of a small screw driver. A scope should be connected to TP7 at the top of board.



Procedure for Amplifier

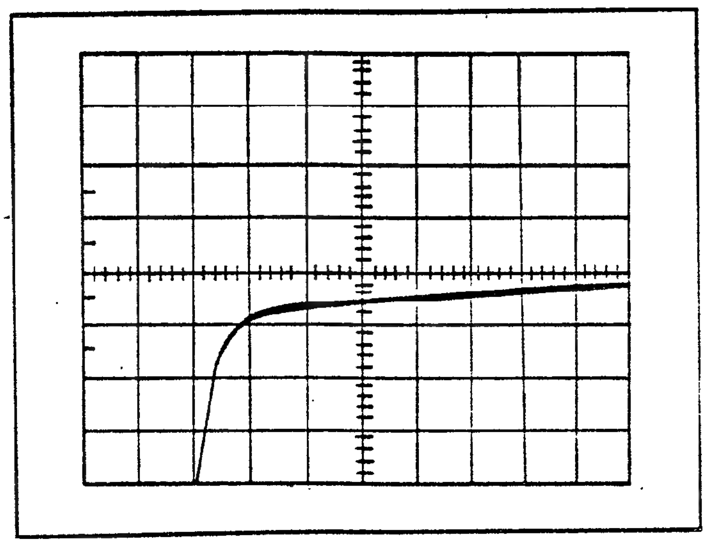
1. Set Coarse and Fine Gain to approximate setting for detector.
2. Set scope for 100 mv/div vertical and 5 μs/div horizontal.
3. Monitor TP9 and if necessary adjust RV7 with random input to detector.

Correct



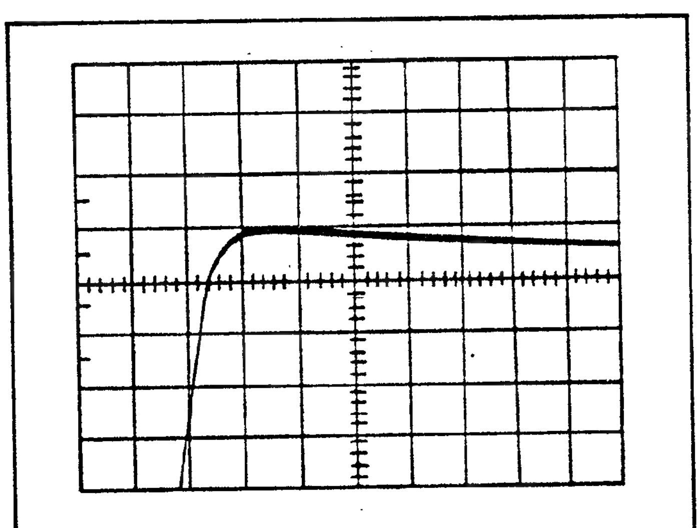
100mV/Div 5μs/Div

Incorrect



100mV/Div 5μs/Div

Incorrect



100mV/Div 5μs/Div

When using the internal amplifier the INPUT switch (S27) must be in the AMP position and the INPUT POLARITY switch (S28) must correspond to the polarity of the input pulses to the amplifier. The bipolar amp performs well to count rates in excess of 50K counts per second.

5.3.1.2 SCA

The SCA sets a window on the ADC input signal. The lower limit is set by the LLD, while the ULD sets the upper level threshold. Both are independently adjustable from 0 to 110% of range. If a pulse falls within this window, a logic pulse is generated at a rear panel connector.

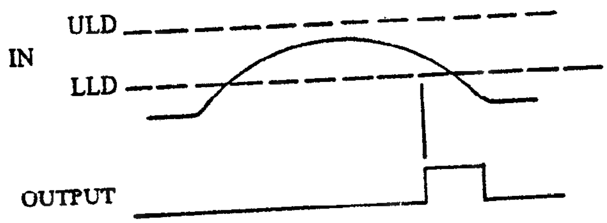


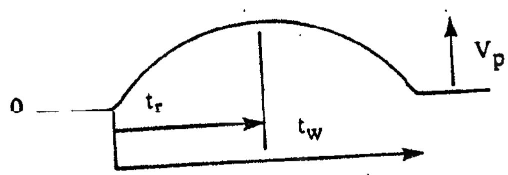
Figure 5-1
SCA Timing

5.3.1.3 ADC GENERAL

The function of the ADC is to convert the input signal to a digital value proportional to its amplitude. The ADC in the 4100 does this by precisely charging a capacitor (stretcher) to the amplitude of the input. Then a second capacitor is charged, linearly, to the same value. During the time the second capacitor is being charged, a crystal-controlled pulse train is counted in a register. This results in the register number representing the height of the input signal. The number is used to select a memory location which is incremented. In Live Display the ADC output positions the CRT beam.

5.3.1.4 ADC IN

The ADC requires positive unipolar pulses, or bipolar (positive going at leading edge) pulses as input. The amplitudes may range from zero to +12 volts. The rise time must be greater than 250nsec and less than 30 microseconds. Longer rise time pulses can be accepted by changing C38 (1000 pf) on the ADC. The polarity and gain controls can be put to their proper settings by using the ADC in PHA-Collect. The polarity position which causes spectrum peaks to fall in higher channels is correct. The Amp gain should now be adjusted for the desired resolution.



$0 \leq V_p \leq +12V$
$0.25\mu sec < t_r < 30\mu sec$
$1\mu sec < t_w$

Figure 5-2
ADC Pulse Input Requirement

.3.1 ADC GAIN

[The ADC Gain controls the resolution of the ADC; i.e., the number of pieces into which a 10 volt nput signal can be divided.

Gain division is made digitally between the 256, 512, and 1024 gains. At 2048 gain the digital factor is the same as 1024 gain and the constant current controlling the ramp capacitor is changed. The digital range (overflow) of the ADC is determined internally by the size of the memory and the setting of the Memory Control switch:

Memory Control	Range for Memory Size		
	256	512	1024
Full	256	512	1024
1/2, 2/2	128	256	512

The percent dead time is indicated by the ADC DEAD TIME % meter on the front panel. This is most useful in comparing count rates of similar spectra.

5.3.1.6 ADC BASELINE

The Baseline controls of the ADC (Zero and Digital offset) vary the intercept of the ADC conversion function. Their effect is to slide the spectrum in the memory (left or right). See the Baseline figure for examples. The Zero is used as a fine adjustment when it is necessary to have a particular peak have its cei id at a predetermined channel address. The factory setting puts ADC for zero energy in channel zero with 1024, 512 or 256 gain; the zero for 2048 may be slightly off. The Digital Offset makes precise shifts of the spectrum. Because of noise and non-linearity problems associated with this general type of ADC, the lower 2% of the input range is not usable. With Digital Baseline, the zero can be suppressed, allowing the entire memory to be used.

Another advantage of Digital Baseline is when taking high resolution spectra in a small memory. For example, if a Ge(Li) detector is used with a 256 channel memory for a gamma ray experiment, it would normally be run for the highest resolution to allow accurate separation and determination of peak positions; by using the Digital Offset, any part of the spectrum can be stored in memory groups as small as 256 channels.

The following calibration procedure is necessary when the Zero control is to have channel zero correspond with zero energy.

1. Connect a Model 8210 Precision Pulse Generator or equivalent to the ADC IN jack.

2. Set ADC Gain to the 1024 or 2048 position. For 256 and 512, the Zero should be set at 1024 gain.

3. Set Memory Control to 1/1.

4. Put Analyzer in PHA Collect. Using Dynamic and moving the cursor will aid in the set-up.

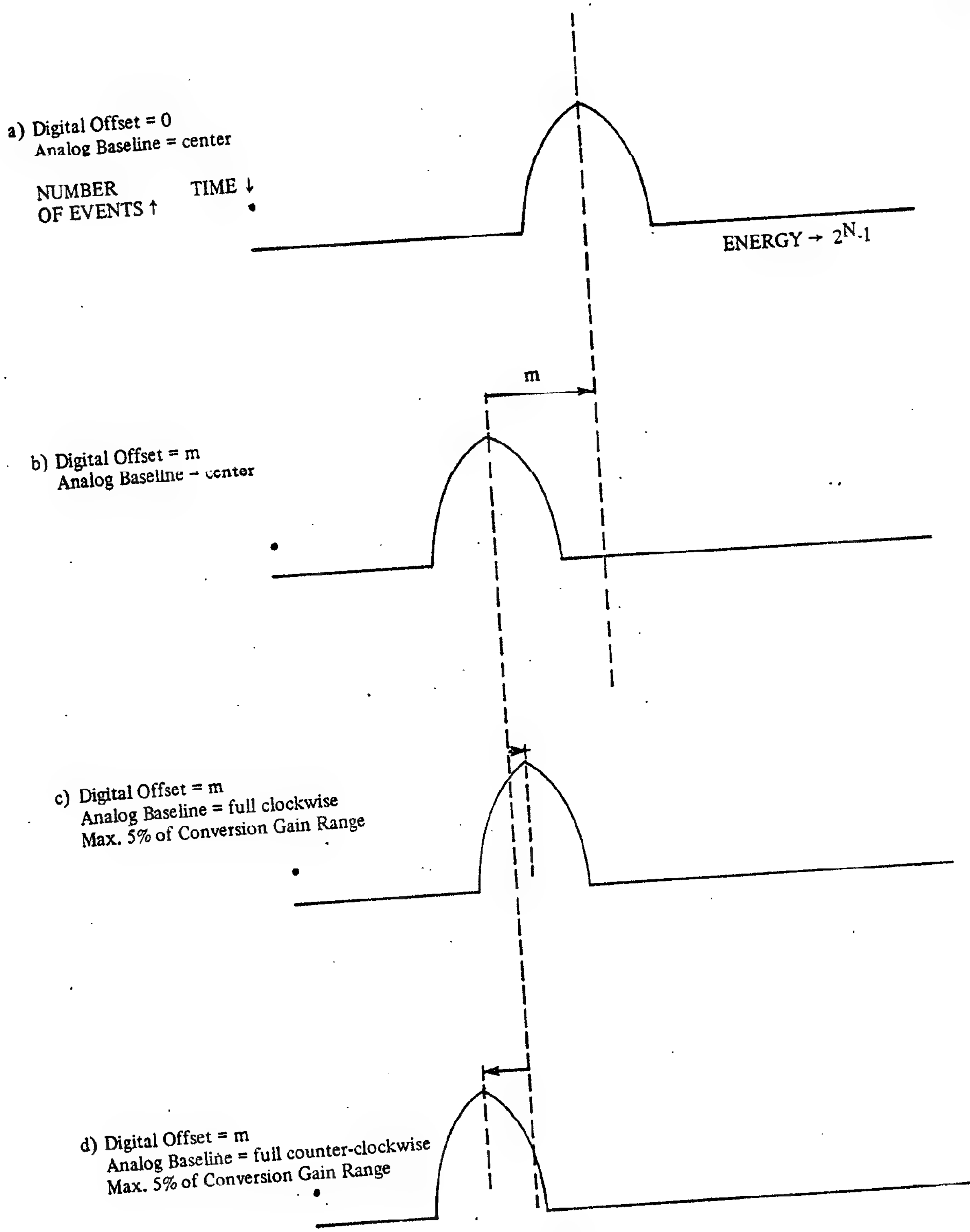


Figure 5-3
Baseline Variation - Examples of Effect on Spectrum

5. If Gain setting is greater than the memory, add sufficient Digital Offset to allow storage in memory. For example, 256 channel memory and 2048 Gain, set Digital offset to 1792 (1024 + 512 + 256).

6. Set all Binary switches on the pulser to the ON position and adjust its Coarse and Fine Amplitude pots for maximum conversion (1023 or 2047). For 256 channel memory, 2048 Gain, and 1792 channels of Offset, this would be at channel 255.

7. Set the most significant 5 toggle switches on Pulser to OFF and set the ADC Digital Baseline to zero. For optimum intercept calibration, the ADC should be converting at:

Gain 2048	Channel 63
Gain 1024	Channel 31

If not, adjust the ADC Zero control.

8. Repeat steps 5-7 until no further adjustments are necessary to Pulser amplitude or ADC Zero pots.

5.3.1.7 ADC COINCIDENCE

Coincidence functions are used to gate the processing of the linear input signal. The ADC has provision for early or late coincidence and anti-coincidence. The analyzer is shipped with the jumper in "LATE". With no input connected to Gate In, conversions are enabled regardless of the Gate switch or jumper positions. Late Coincidence requires the LATE jumper installed on the ADC; the Gate switch set to COINC; and a positive logic pulse applied to GATE IN during Linear Gate time. Linear Gate time is variable. It is normally initiated by the input crossing the LLD threshold and normally terminated by the peak sense logic. If no pulse is received, the ADC logic will reset the stretcher capacitor and logic making it ready for another input.

Early Coincidence requires moving a jumper on the ADC from the sockets marked LATE to those marked EARLY; the Gate switch set to COINC; and a positive logic pulse applied to GATE IN at the time the Input signal crosses the LLD threshold. Early coincidence is preferable when a high count rate is being gated because of the added dead time introduced in Late. However, Late Coincidence gating is easier to do since a delay amplifier is not needed. The added cost and degradation of the linear signal by the delay amplifier must also be considered. In either of the coincidence modes only one jumper, Early or Late, should be installed.

Anti-Coincidence has the same requirements as Coincidence experiments, except that the gating pulse prevents a conversion instead of allowing one.

5.3.1.8 SAMPLE VOLTAGE ANALYSIS

Analog voltages (DC or slowly changing AC voltages) can be sampled by the ADC in the Model 4100. The result will be an amplitude distribution curve. The ADC Input must be used because the internal amplifier is designed for pulse amplification. The input signal must be a 0 to +10 volt signal. The SCA window is used to allow conversion of signals which are between the LLD and ULD settings. The GATE input (J1, J103 on rear panel) supplies the sampling signal (> 250nsec width).

The analyzer is operated in the Coincidence mode; PHA; and requires the SAMPLE Jumper installed. EARLY and LATE Coincidence jumpers are removed.

5.3.1.9 PHA PRESETS

To end the Collect state, it is frequently convenient to use a Preset Timer. A Preset Timer is built into the analyzer which can be set to record Live Time at settings from one second to 900,000 seconds (Or 250 hours). The time is accumulated in Channel Zero of the Memory group used and can be seen as it is stored. Time will always be added, never subtracted, and can be reset in Display by depressing the Channel Zero switch. An External Preset can also be used and is brought in through a rear panel BNC. When the Preset is reached, the Collect state will end. With the I/O Cycle switch in Manual, the analyzer goes into the Display state. If the I/O Cycle switch is on Single or Recycle, the data will be read out to the selected device. In Single, after readout, the analyzer goes into Display without affecting the data; in the Recycle position, the data will be reset after readout and the analyzer returns to Collect more data. (External Preset is Collect Stop, J109, on rear panel)

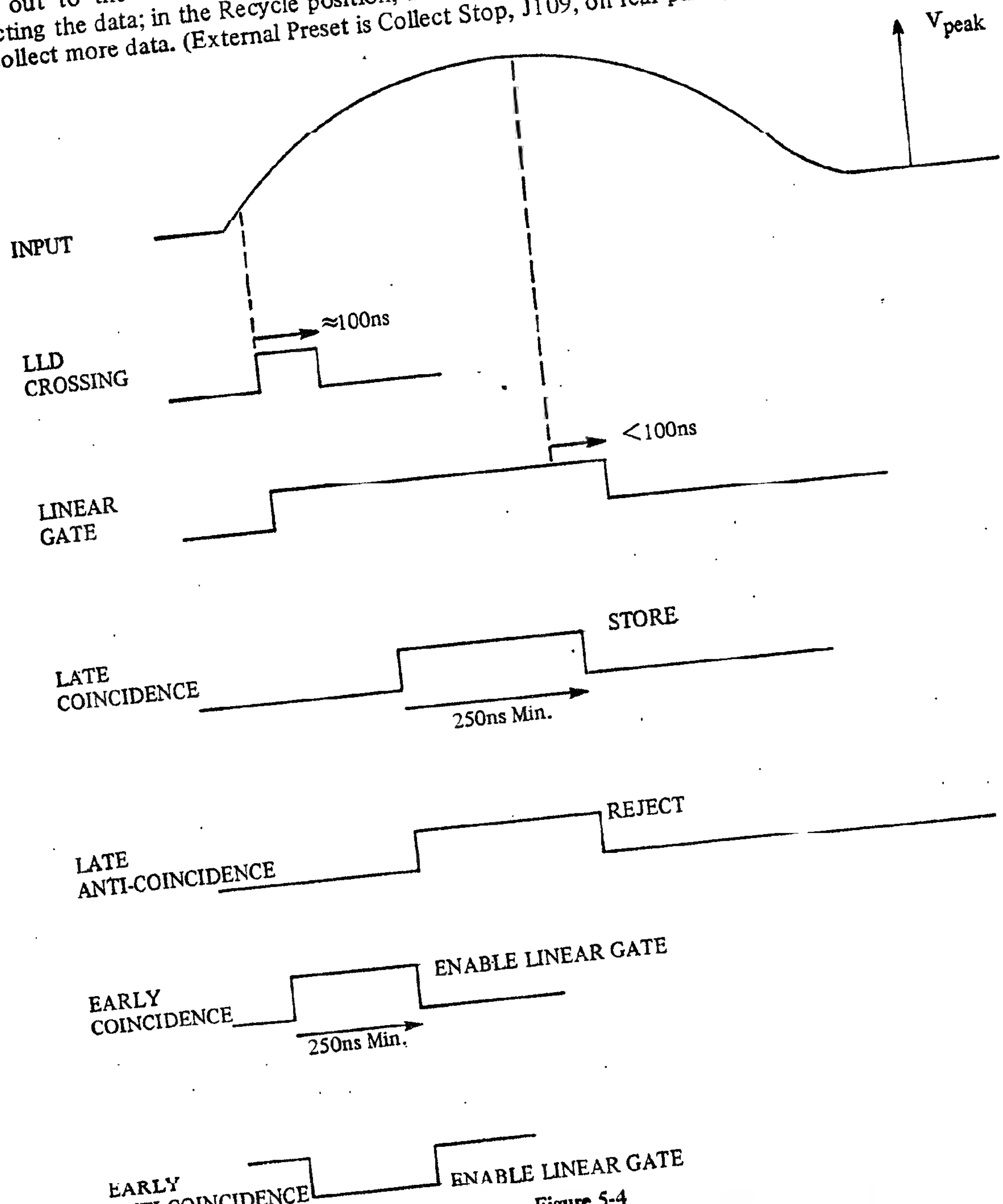


Figure 5-4
Gate In Timing

5.3.2 MULTISCALING

When multiscaling, the number of occurrences as a function of time is recorded in the memory. The time per channel, or dwell time, can be determined by the internal timer or from an external generator. Set Preset Time to 00 when using an external generator. The input to the multiscaler is a logic pulse. The number of pulses per unit time in a window within the spectrum can be recorded using the SCA. Since the SCA operates on the input to the ADC, using the PHA mode greatly aides in determing where this window is. It can be set by putting the analyzer into PHA Collect and adjusting the window around the peak of interest. The SCA LLD "edge" is much sharper than the ADC because the ADC must store on a stretcher the pulse that triggers the Lower Level.

The maximum input rate to the Multiscaler is 10 MHz. The minimum pulse width (positive) requirement is 50nsec. measured at 1.5 volt amplitude. Narrower pulses will not be counted correctly The SCA should be used to shape slow logic pulses since the maximum pulse width for the count input is 800 nanoseconds. The Multiscale dwell time is determined by the preset timer in the control section of the analyzer. It can be set from 100 microseconds to 0.9 seconds. It is always true time (live time is measured in PHA). The time required to carry out a full Write-Address Advance-Read cycle for a memory location is 24 microseconds During this time the Analyzer is "dead" and will not accept COUNT IN pulses. If a single sweep is desired the CONTROL switch should be placed in the MCSS position. For multiple or recurring sweeps, it should be placed in the MCSR position. Whether the count input is added, subtracted, or does not change the contents of the memory, is the function of the Control ADD-OFF-SUB switch. Additional features provided for external control are a Sweep Trigger input (TRIG IN J106); a Sweep Out pulse (SWEEP OUT J108); and a Collect Stop input COLLECT STOP J109). The Sweep Trigger input provides a means in the MCSR or MCSS modes, to initiate the sweep remotely. The Sweep Out pulse indicates the beginning of each sweep and is useful for counting the number of sweeps by an external counter. The Collect Stop input allows a logic pulse ut, during a sweep, to cause the experiment to end at the end of the sweep in progress.

When Collect is enabled for Multiscale, the CRT displays each channel before it is modified by the memory cycle. Therefore, the display is one sweep behind in data (vertical deflection). During a single sweep experiment the data collected would not be seen until the experiment was finished and the analyzer was in Display.

5.4 READ OUT

5.4.1 GENERAL

Read Out provides the method of recording information from the analyzer. Several analog and digital devices can be used with the Model 4100. With the Control MAN-SINGLE-RECY switch, repetitive cycles can be generated. The Control DIGITAL-PLOT switch allows a choice between the standard analog read out to a plotter or an optional digital read out to one of several available devices. The optional devices include TTYs, Printers, RS 232 compatible devices (such as Modems, terminals and computers), and Canberra Scanners. Refer to the appropriate Appendix for operation, format and installation details for each of the options.

An I/O Serial Interface (option series 15) has been developed for later units. Units with the "15" options will have the Read Out state button replaced with an I/O button and the lower front panel Digital/Plot switch replaced with a Digital Out/In/Plot switch.

These interfaces may be used in a system which also has a Model 2089 Printer connected. The Printer ON-OFF switch providing the control necessary to disable the Serial Interface.

See the appropriate appendices for complete description of the option 15's.

5.4.2 CYCLES

Setting the Control switch to MAN provides manual control of Read Out. If allowed to proceed to the finish, Read Out will terminate and the system will place itself into the Display state. The SINGLE position provides for entering Read Out automatically at the end of Collect. If allowed to proceed to the finish, Read Out will terminate and the system will place itself into the Display state. The RECY position provides continuous cycling between Collect and Read Out. When Collect terminates, the system will enter Read Out. As data is read from each location, the memory is reset to zero. When Read Out terminates, the system is automatically placed into Collect. This sequence will continue until the RECY position is changed to SINGLE or MAN, or Read Out is terminated by manually pressing the Read Out switch. The experiment may be terminated manually at any time the analyzer is in Read Out of it in Collect by pressing Collect and Read Out simultaneously. The analyzer will then be in the Display state.

5.4.3 SELECTIVE*

It is possible to transfer all the information in the Memory Group or only that in the selected area of it from the Analyzer to the read out device. With Intensify OFF, all the data in the group determined by the Memory Control switch will be transferred. For selective read out, set Intensify ON; data in Channel Zero and in the region-of-interest (defined by Cursor locations) will be transferred.

Limitation - When placing the system into the Readout state with Intensify ON (selective Readout) the following should be observed in order to attain the proper output format. Do not place the Stop Cursor equal to the Start Cursor.

5.4.4 INTEGRATE*

With Integrate ON, the summation of data in the region-of-interest is calculated and recorded. The format is designed to print the Start and Stop addresses of the ROI. With Intensify OFF, the ROI has a start channel of 1 and a stop address equal to the number of channels in the Memory Group (e.g., 128, 256, 512, etc.). Normally, data is also read out, providing the count information for each channel integrated. To read out only the integral word, change a jumper on the Basic Read Out card from BC to AB. With Integrate OFF, the function is disabled, and memory data in the ROI will be transferred.

5.4.5 DATA MODULES*

The analyzer is designed to be used with Canberra Data modules. These can be Scalers, Tagword Generators, or a Canberra Scanner, such as the Model 1487 Paper Type Scanner. The data in the Modules is always read out before the analyzer data, and is identifiable as tag words.

If a scanner is to be used to interface to the recorder, any interface board in slot 1A must be removed.** If the analyzer controls the Readout device, a scanner cannot be connected and an interface board must be in slot 1A. In the Daisy Chain the analyzer acts as a master.

1. Reset
   a. Resetting analyzer data (Manually or in Recycle) clears the modules.
   b. Pushing Reset on a Master module will clear other modules but have no effect on analyzer.

2. Start
   a. Going into Collect starts all modules.
   b. Starting a Master module will set the analyzer into Collect.

3. Stop
   a. Ending Collect stops all modules.
   b. Reaching a Preset in a Master module ends Collect.
   c. Pressing Stop button on Master module ends Collect.

If data is to be read out through the analyzer, the Read Out controls operate normally. With the scanner (Models 1486, 1487, etc.), the read out can be started manually only by pressing Read Out on the Model 4100. Several automatic cycles can be performed.

1. If all the data in the analyzer and the modules is to be reset before collecting resumes, the analyzer must be in RECY and all the modules (including the scanner) must be in Single Cycle mode.

2. If the analyzer data is to be cumulative (that is, not reset between cycles), then the Model 4100 should be set to SINGLE and one or more of the modules must be in Recycle. In this cumulative oode, the analyzer Preset Time switch should be set to 00.

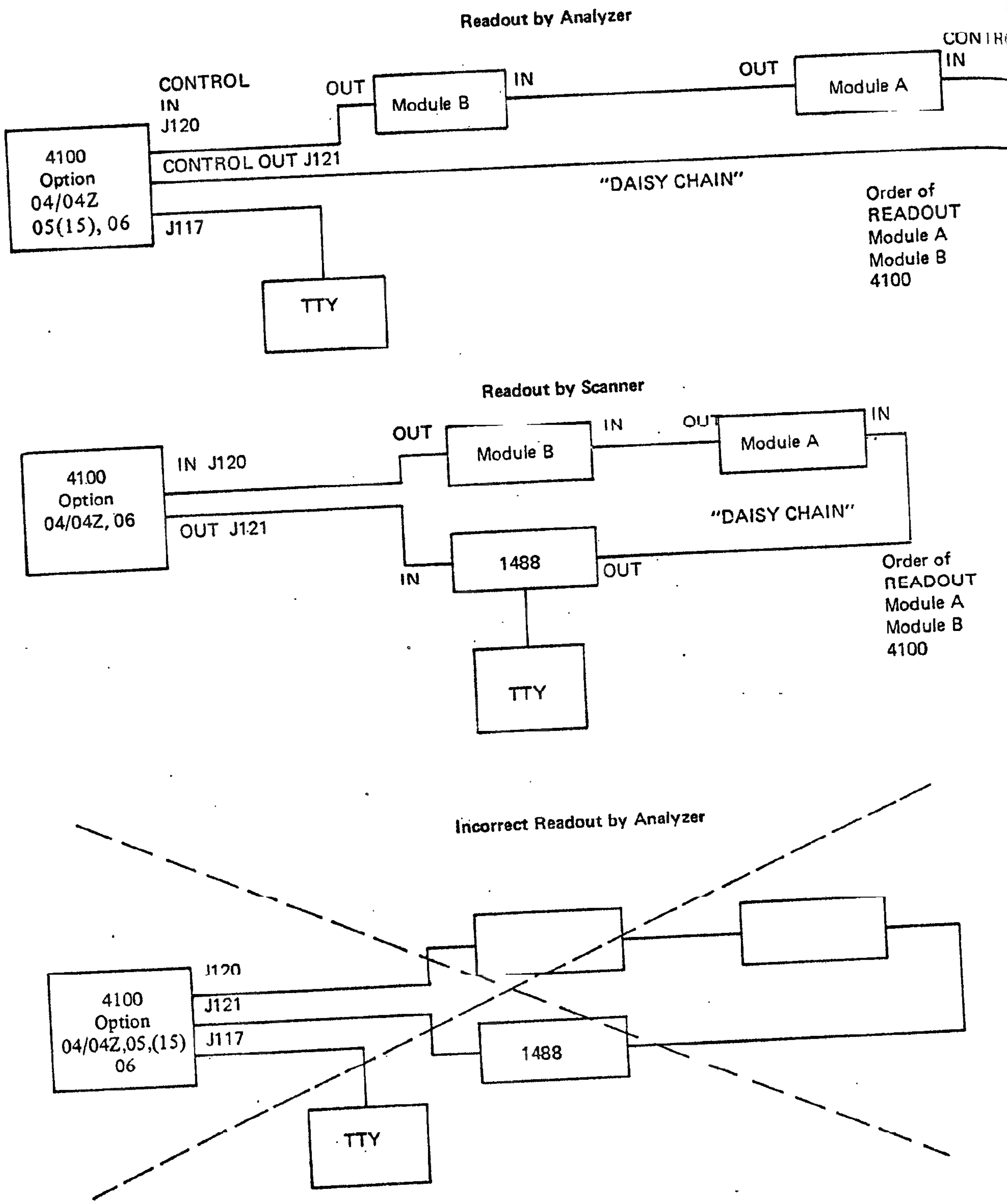


Figure 5-5
Readout Block Diagram

Section 6
USER'S GUIDE

6.1 GENERAL

This section is intended to provide the user of an OMEGA-1 Portable MCA with the information necessary to install and operate the OMEGA-1 in a normal laboratory environment. In addition, several common experimental procedures will be outlined to facilitate system setup. It is assumed that the user has the following equipment available for use:

Model 4100-C OMEGA-1 MCA (1024 Channels), with the following options:

Model 4100-02 Data Analysis Option

Model 4100-03 Detector Bias Supply

Model 802-3 2" x 2" NaI detector with PM Tube

Model 802-9 Tube Base and Preamp

Assorted Cables

Assorted Calibration Sources, including Cs-137, Co-60, Co-57

6.2 PULSE HEIGHT ANALYSIS (PHA) INITIAL SETUP

Operation of the Omega-1 as a Pulse Height Analyzer, will be used to describe the basic characteristics of the unit since it is the most common application and requires the use of a large majority of the controls and features.

Using the components listed in Section 6.1 connect the system as shown in Figure 6-1.

6.2.1 SWITCHSETTING

After interconnecting the various components, set the following switches as indicated:

FRONT PANEL

MEMORY CONTROL: FULL
PRESET TIME: 00
STRIP/COMPARE/OFF: OFF
INTEGRATE: OFF
INTENSIFY: OFF
CURSORS: STOP
DISPLAY: LIVE
GATE: ANTI
INPUT: AMP

LOWER PANEL

POWER: OFF
VOLTS: 0 (Coarse and Fine)
MCSS/MCSR/PHA: PHA
RECY/SINGLE/MAN: MAN
SUB/OFF/ADD: ADD
DIGITAL/PLOT: Not Applicable
LLD: 0.2
ULD: 10

INPUT POLARITY: POS
COARSE GAIN: 30
FINE GAIN: 50
GAIN: 1024 OFFSET:
OFFSET: ALL SWITCHES DOWN

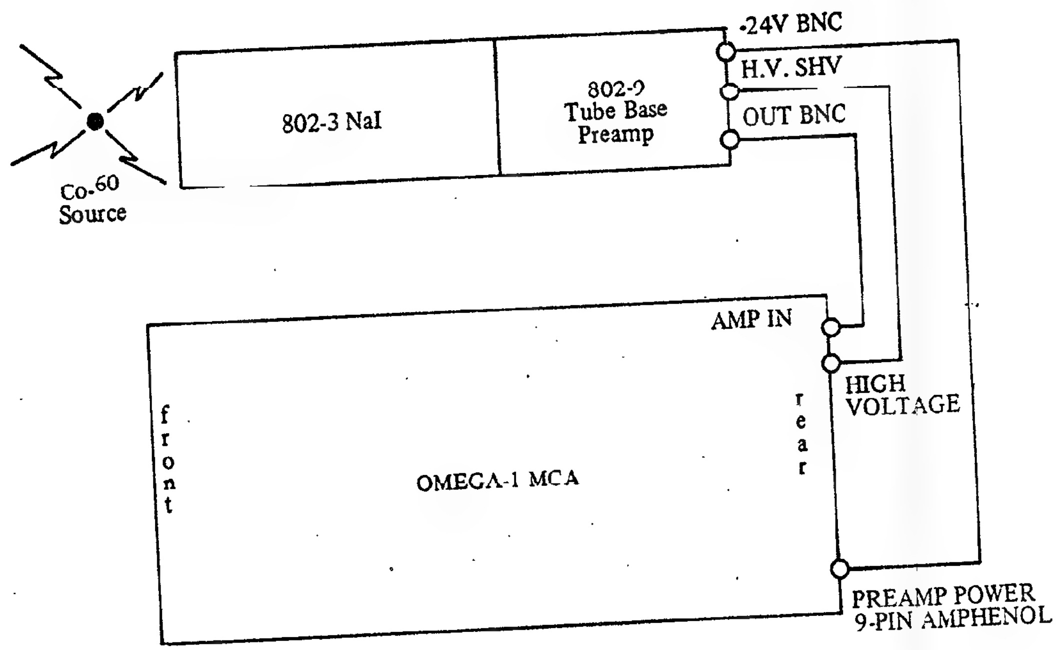


Figure 6-1
PHA System Setup

Once the above controls have been set, turn POWER ON and verify that the + indicator on the High Voltage Power Supply is illuminated. (Refer to Appendix B of the manual for instructions on changing the polarity if required.)

After allowing a few minutes for warm-up, set the VOLTS control to 1000 and depress the COLLECT pushbutton. Using the CRT "Picture Control" (Intensity, Gain, etc.), you should now see a LIVE–each pulse displayed as it is stored–display on the CRT, indicating proper system operation. By flipping the DISPLAY switch from LIVE to DYNAMIC, a static display of the incoming data can be seen.

6.3 ENERGY CALIBRATION

Once proper operation has been observed, the energy calibration process can be performed. By establishing a direct relationship between photopeak energy and MCA channel number, the task of identifying unknown isotopes can be greatly simplified.

Assuming a desired energy range of approximately 0-2MeV (2keV per channel) the process is as follows, and illustrated in Figure 6-2:

A. Place CURSORS switch in the STOP position. This enables movement of the rightmost cursor. The MCA should be stopped (COLLECT and READOUT off).

B. Move the SCAN control to the right until the STOP cursor is in channel #666 (1322 keV/2).

C. Place the CURSORS switch in the START position, enabling the leftmost cursor.

D. Move the SCAN control to the right until the START cursor is in channel #61 (122 keV/2).

E. Place a Co-57 and Co-60 source near the detector, and begin collecting a spectrum in DYNAMIC display

F. Adjust the amplifier gain (occasionally RESETTING memory if needed) until the Co-57 peak at 122 keV and the Co-60 peak at 1332 keV are in alignment with the START and STOP cursors respectively. Note that this is an iterative process and may require a slight adjustment of the ADC Zero to achieve an accurate alignment.

Once this procedure has been completed, qualitative analysis is greatly simplified, since energy is directly equal to 2 x Channel #.

6.4 EFFICIENCY CALIBRATION

Once the energy calibration has been completed, qualitative analysis is relatively straightforward. To proceed from qualitative to quantitative analysis, however, requires calibrating the system for efficiency as well as energy.

Since a detector's efficiency is really just a ratio of events observed versus events which actually took place, it is extremely important that accurately calibrated sources be available. Secondly, detector efficiency varies with energy. This requires many different, accurately known sources if a complete efficiency versus energy curve is to be developed for a given detector at a given source to detector geometry. While the procedures which follow will use only one photopeak, they can be applied to all the various peaks which must be used to produce an efficiency curve.

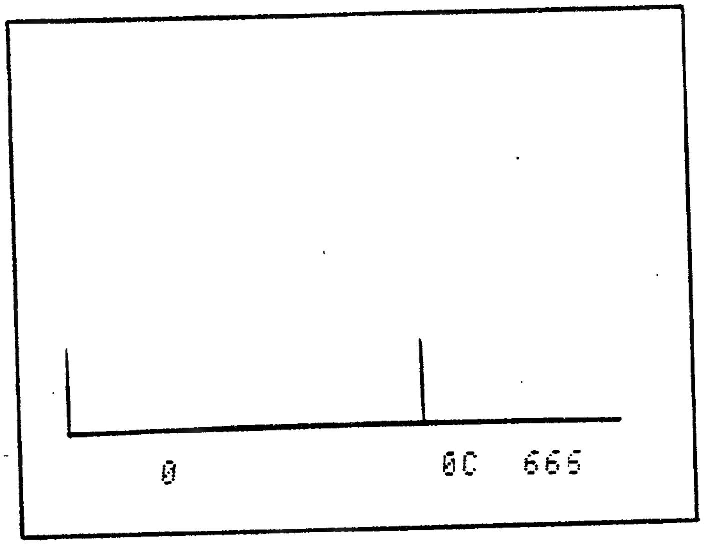


Figure 6-2a
STOP Cursor at Channel 666

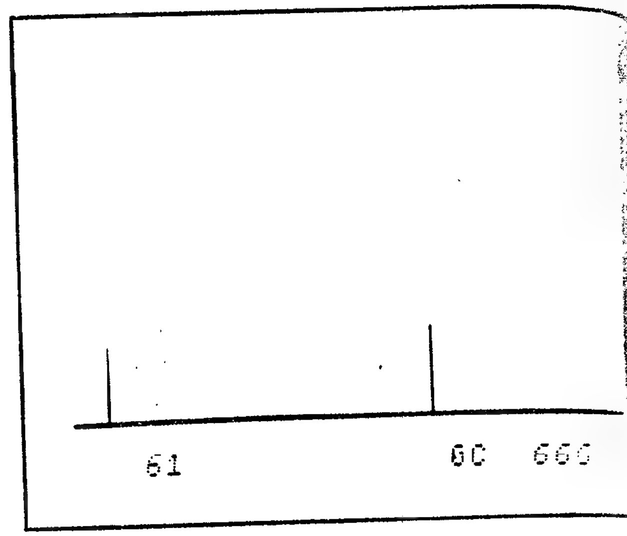


Figure 6-2b
Both START and STOP Cursors in position

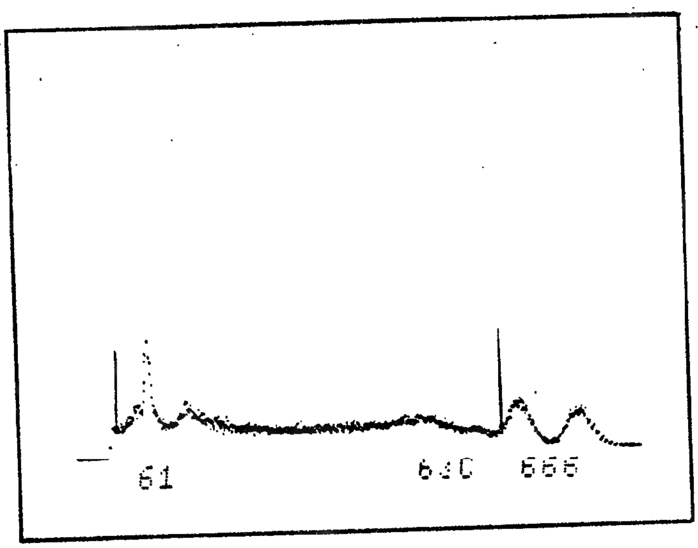


Figure 6-2c
Spectrum prior to gain adjustment

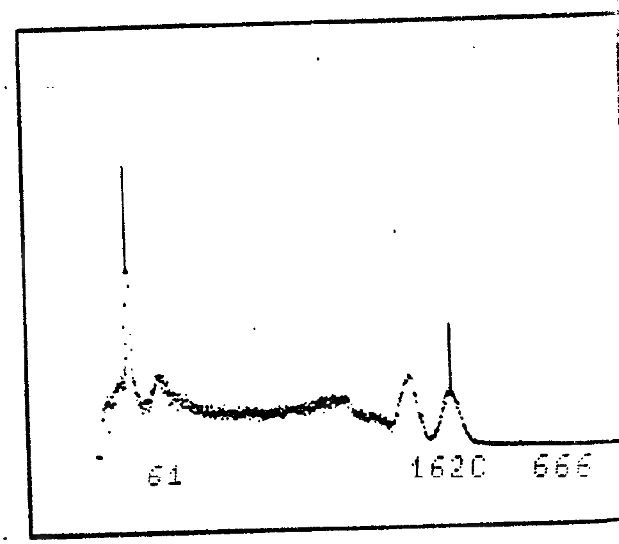


Figure 6-2d
Properly calibrated system

Figure 6-2
Energy Calibration Procedure

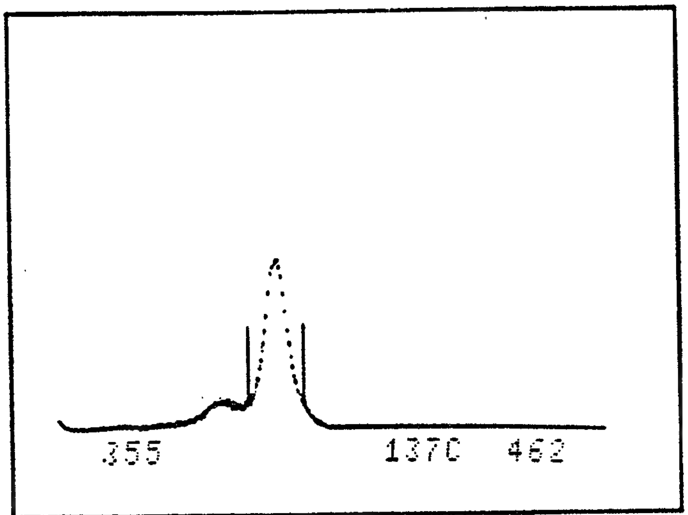


Figure 6-3a
Peak "bracketed" with the Cursors

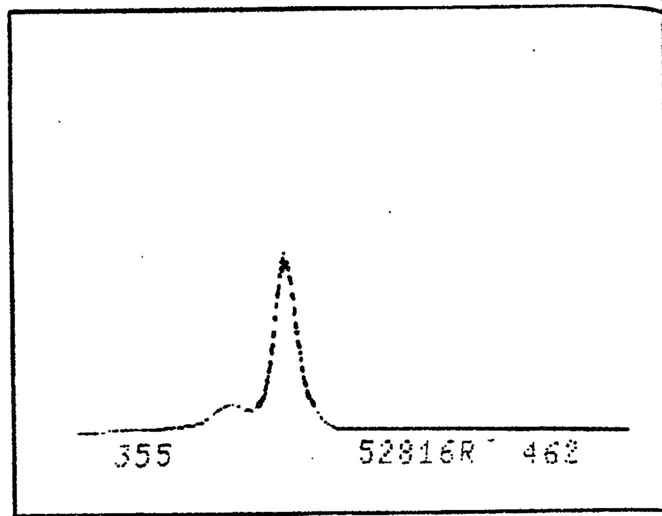


Figure 6-3b
INTENSIFY and INTEGRATE yield the integral of the region

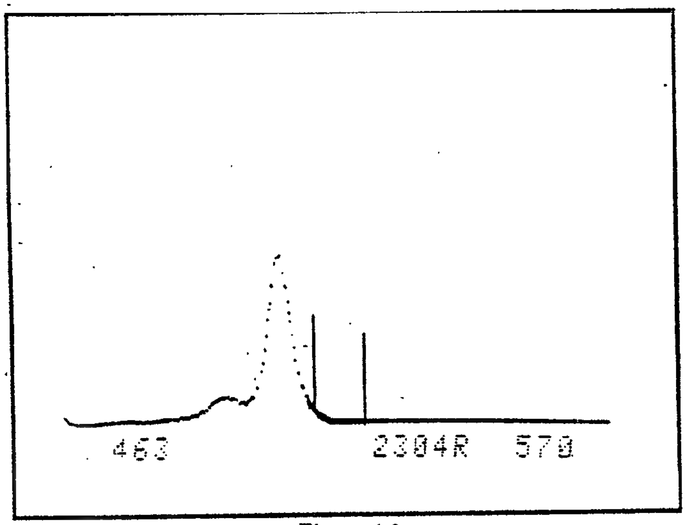


Figure 6-3c
Measuring the low energy background

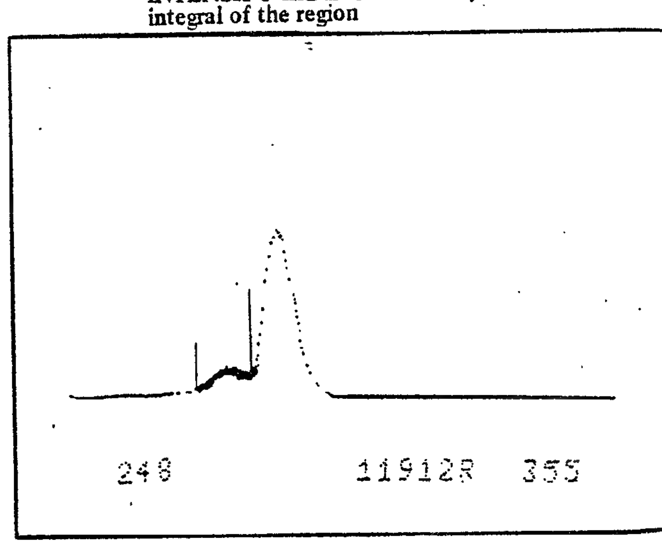
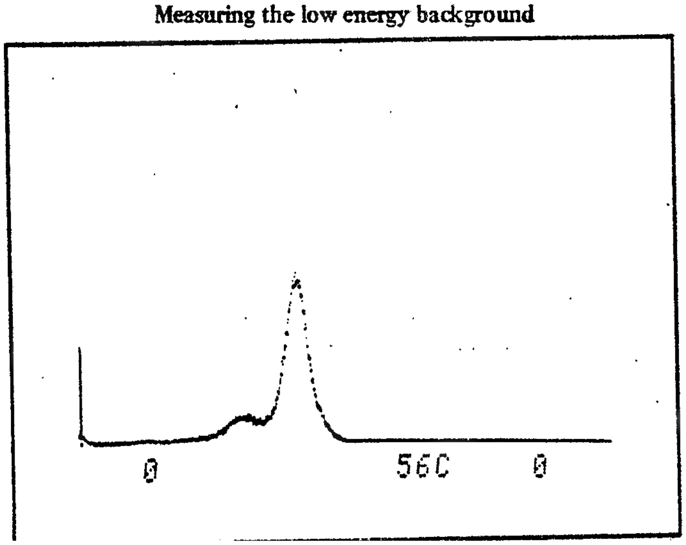


Figure 6-3d
Measuring the high energy background



6.5 ISOTOPIC ANALYSIS

A ,entioned in previous sections, the qualitative - or isotope identification - portion of spectrum analysis is easily performed once energy calibration has been completed. In general it simply involves determining the energy of photopeak, via the cursors, and using a table of isotopes to determine the possible sources of the peak. Intuitive knowledge of the sample contents, plus cross checking for secondary peaks, can be used to verify a tentative identification.

Once an isotope has been identified, a procedure similar to that used in efficiency calibration is used to take the data needed for quantitative analysis.

6.5.1 TAKING THE DATA

The data needed for quantitative analysis are Peak Integral, Low Background, High Background, and Live Time. These values should be measured and recorded exactly as described in section 6.4.1, steps A-H.

6.5.2 COMPUTING SAMPLE ACTIVITY

The following procedure details the computation:

A. Peak Area = Peak Integral - (Low Background + High Background)/2

B. Current Activity (μCi) = .00027 x $\dfrac{\text{Peak Area}}{\text{Live Time x Efficiency x Yield}}$

Note that the Efficiency number is from a previous efficiency calibration run, and that the Yield is from a table of isotopes.

C. Quite often it is necessary to perform a decay correction back to some t_o.

The process is:

$$\mu\text{Ci@To} = \mu\text{Ci} \times e^{\frac{.693 \times \text{Decay Time}}{\text{Half Life}}}$$

Note that the Decay Time and Half Life must be in the same time units.

6.6 ANALYSIS BY COMPARISON

Due to the relatively poor resolution characteristics of a NaI(T1 detector, chemical separations are often performed on a complex sample to simplify the analysis. If these separations yield sub-samples which contain essentially only one isotope, the COMPARE function of the OMEGA-1 can greatly simplify the analysis.

To use this technique requires that two separate spectra be taken; a reference in one half of memory and the unknown in the other half. For this method to be successful, it is very important that:

A. The current activity of the reference standard be accurately known.

. The reference standard be of the same geometry as the unknown sample.

C. The collect time of the two data acquisition runs be exactly the same.

Steps B & C are simply to establish constants; if B & C are constant, the only differences between the two spectra will be due to differences in activity.

6.6.1 COLLECTING THE DATA

A. Place the reference standard in position for data acquisition.

B. Establish a suitable Preset Time via the thumbwheel switches.

C. Set the ADC Gain to 512, the Memory Control to 1/2, and Reset memory.

D. Collect a spectrum, and wait until completion.

E. Remove the reference and place the unknown in position.

F. Set the Memory Control to 2/2, and Reset memory.

G. Collect a spectrum, and wait till completion.

H. Set the Memory Control to FULL. Two identical spectra, differing only in amplitude (activity) will be seen on the CRT. See Figure 6-4a.

6.6.2 MAKING THE COMPARATIVE ANALYSIS

Figure 6-4 and the procedure below details the steps required to complete the comparative analysis.

A. Set the Memory Control to the smaller (lower in amplitude) half of memory. In the example this will be 2/2.

B. Adjust the % potentiometer to 100% (full scale).

C. Set the COMPARE/STRIP/OFF switch to COMPARE. Note that the two spectra are now overlapped on the CRT.

D. Using the % potentiometer as an attenuator, and Vertical Bias control for positioning, adjust the display until the two spectra are identical.

E. The setting of the % potentiometer is the ratio – from 0 - 100% – between the sample and the standard.

6.7 BACKGROUND SUBTRACTION AND SPECTRUM STRIPPING

Depending upon the application, there are two methods of "stripping" available on the OMEGA-1. For background subtraction, true subtraction is normally used; for reference stripping the visual STRIP is most common. Both are described in the following sections.

6.7.1 BACKGROUND SUBTRACTION

True background subtraction is best accomplished by using the Subtract, rather than Add, mode of data acquisition. While this is somewhat limited in capabilities - especially in comparison to the Model 8180 MCA - it does provide very accurate results when properly performed. Figure 6-5, and the procedure below, detail the operation.

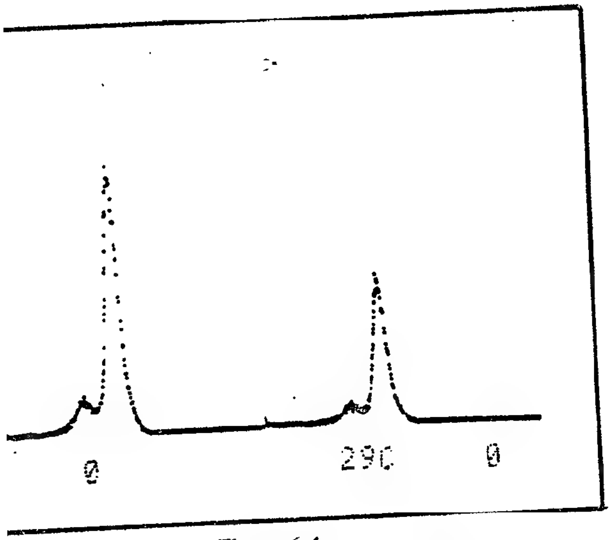


Figure 6-4a
Left half contains the standard right half the unknown. Memory Control set to FULL.

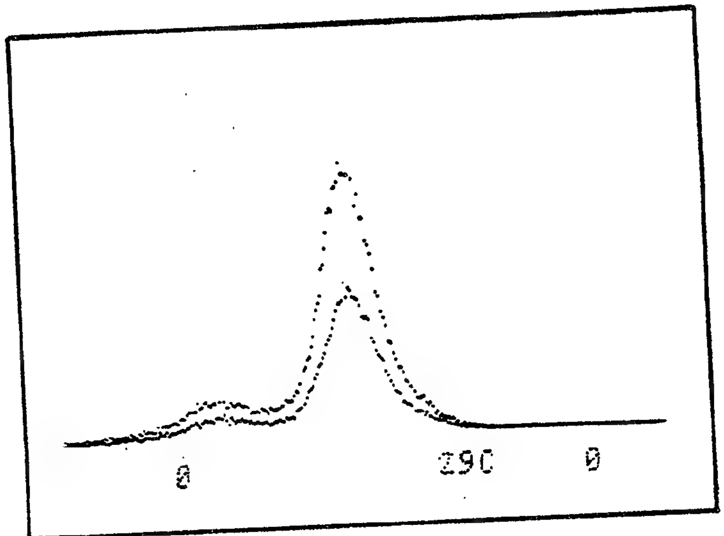


Figure 6-4b
COMPARE enabled. Memory Control set to 2/2.

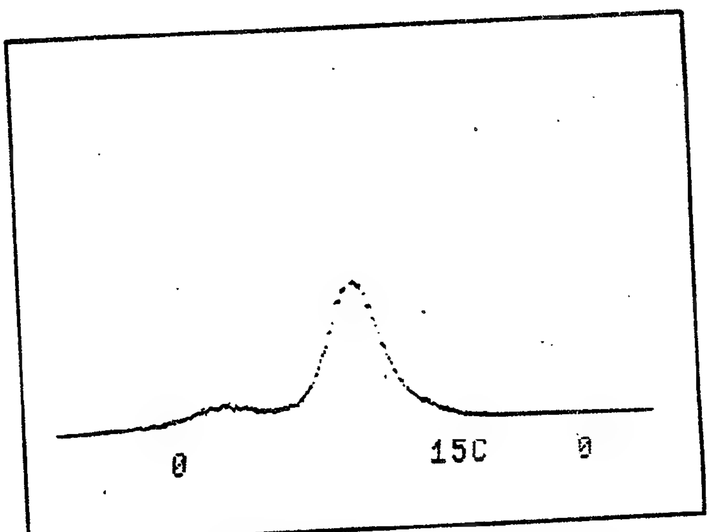


Figure 6-4c
CRT display with % and Vertical Bias properly adjusted.

Figure 6-4
Use of COMPARE

A. Set Memory to 2/2, ADC Gain to 512, and CONTROL Mode to SUB.

B. Reset Memory.

C. Remove all sources, in preparation for a background count.

D. Set the Preset Time to the desired value. Note that the same preset time used for this background run must also be used for the sample runs.

E. Collect the background.

F. When the preset is reached, set memory to 1/2 and Transfer. The background data has now been duplicated into the first half of memory.

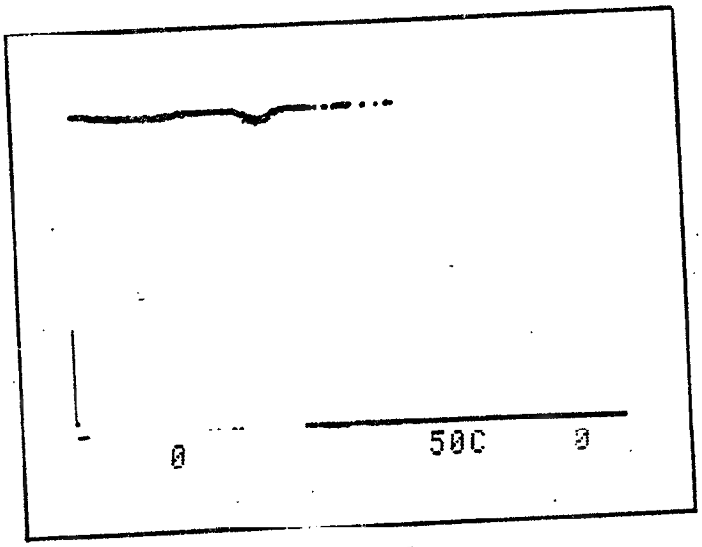


Figure 6-5a
Background Spectrum collected in Subtract Mode.

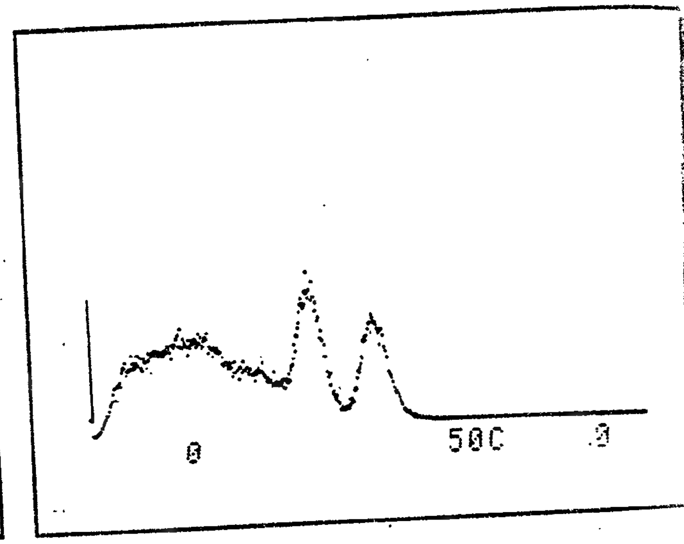


Figure 6-5b
Final spectrum is sample minus background. The "fringe" on the top is caused by statistical variations between the two counts.

Figure 6-5
Background Subtraction

G. Set CONTROL Mode to ADD, place the sample in position, Reset Channel #0 only, and collect a spectrum.

H. When the preset is reached, the first half of memory will contain a background subtracted spectrum.

For each additional sample repeat the procedure starting at step F.

6.7.2 VISUAL SPECTRUM STRIPPING

When a sample contains more than one isotope it is often difficult to make an analysis of the spectrum using the compare function. The Visual Spectrum Strip can be used in this situation.

Figure 6-6 illustrates this use of the Strip function. The procedure used is as follows:

A. Sample spectrum collected in first half of memory.

B. Co-60 Reference Spectrum collected in the second half of the memory.

C. Setting memory control to Full yields a side-by-side comparison.

D. To separate out the Co-60 set the Memory to 1/2, the % potentiometer to 0 and enable STRIP

E. Increase the % value until Co-60 has been visually removed from the sample. Note the % reading to determine the intensity of the Co-60 in the sample.

The Strip can also be used to advantage when it becomes difficult to resolve photopeaks within the resolution of the detector. Subtracting out one of the peaks using strip can be used to verify the presence of an interfering isotope.

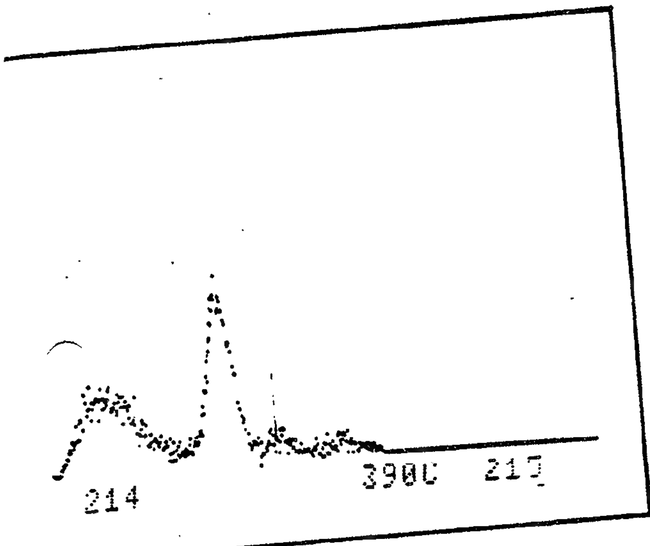


Figure 6-6a
Sample Spectrum in first half of memory.

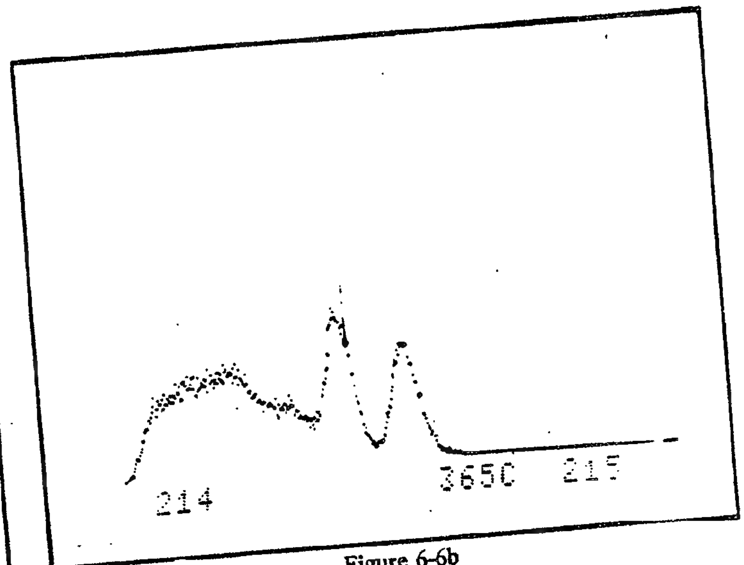


Figure 6-6b
Co-60 in second half of memory.

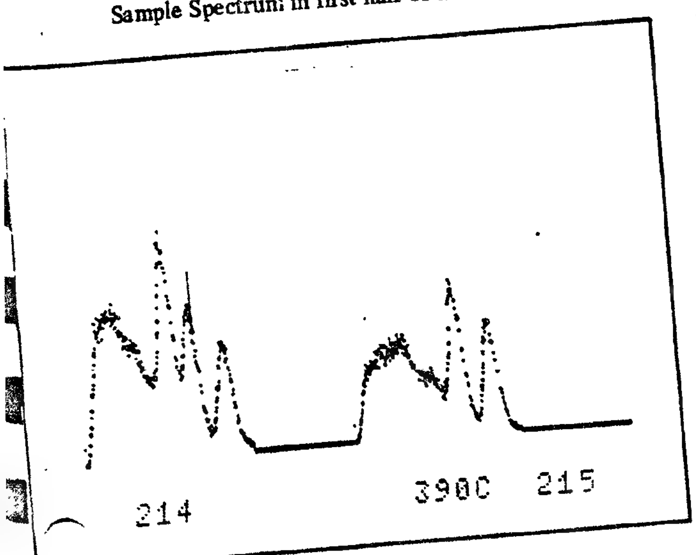


Figure 6-6c
Side by side comparison.

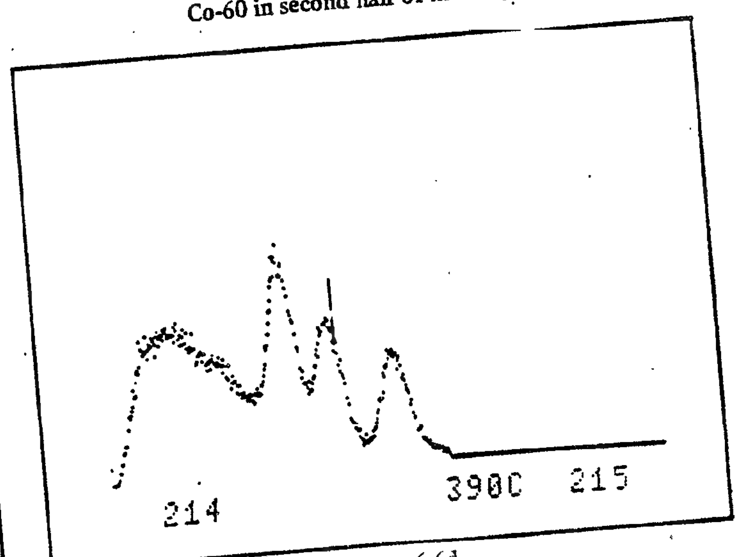


Figure 6-6d
The interferring peak is visible after the Visual Spectrum Stripping.

Figure 6-6
Visual Spectrum Stripping

Section 7
REAR PANEL CONNECTORS

7.1 REAR PANEL CONNECTORS

J101	AMP Input	BNC
J102	ADC Input	BNC
J103	Gate Input	BNC
J104	SCA Output	BNC
J105	Count Input	BNC
J106	Trig Input	BNC
J107	ADV Input	BNC
J108	Sweep Output	BNC
J109	Collect Stop In	BNC
J110	Spare	—
J111	Spare	—
J112	Spare	—
J113	Plotter	25 Pin
J114	Preamp Power	9Pin
J115*	Auxiliary	15 Pin
J116*	High Voltage	SHV
J117*	TTY Out	9 Pin
J118*	EIA Out	25 Pin
J119*	EIA Out	25 Pin
J120*	Control Out	15 Pin
J121*	Control In	15 Pin
J122*	Printer	50 Pin

NOTE: All connectors Amphenol series 17 female except: J119 is a data set equivalent (Cinch DB-19604-433) and is equipped with threaded retaining spaces; J120 is a series 17 male.

7.2 BNC CONNECTORS

	PIN	TO	SIGNAL
J101 Amp Input	1	PC9B-K	AIN
	2	PC9B-J	AINR
J102 ADC Input	1	S27-A3	ADC In
	2	S27-B3	ADC ING
J103 Gate Input	1	PC9A-E	Gate IN
	2	GND	Gate INR
J104 SCA Output	1	PC9B-3	SCA OUT
	2	PC9B-4	SCA OUTG
J105 Count Input	1	PC5A-20	CNT
	2	PC5A-2	GND
J106 Trig Input	1	PC6A-R	Ext Swpt
	2	GND	

*Optional

7.2 BNC CONNECTORS (CONTINUED)

	PIN	TO	SIGNAL
J107 ADV Input	1	PC5A-H	Ext Adv
	2	GND	
J108 Sweep Output	1	PC5A-19	SWPT
	2	GND	
J109 Collect Stop In	1	PC6A-H	COLL STOP
	2		

7.3 J113 PLOTTER (Mating Cable Connector Amphenol 17-20250-1)

PIN	TO	SIGNAL	
2	PC3B-26	X GND	
23	PC3B-S	X PLOT	(0 to +5v)
4	PC3B-26	Y GND	
21	PC3B-19	Y PLOT	(0 to +5v)
5	PC6A-26	SEEK (Out)	(+5) ≈150µs)
6	PC6B-7	CPC (In)	(4V min complete Plot)
9	PC6A-DD	NABL (Out)	(+5 Plot disable 0V Plot enable
14	Mother Board Gnd Bus	GND	

7.4 J114 PREAMP POWER (Mating Cable Connector Amphenol 17-20090-1)

PIN	TO	SIGNAL
1	Mother Board Gnd Bus	GND
2	Mother Board Gnd Bus	Gnd
4	PC1B-17	+12
6	PC1B-R	- 24
7	PC4A-FF	+24
9	PC9A-27	- 12

7.5 J115 AUXILIARY (MATING CABLE CONNECTOR AMPHENOL 17-20150-1)

PINS NOT ASSIGNED

7.6 J116 HIGH VOLTAGE (SHV COAX connector)

PIN	TO	SIGNAL
1	Detector Bias Supply	High Voltage

7.7 J117 TTY (Mating Cable Connector Amphenol 17-20090-1)

PIN	TO*	SIGNAL	
1	R	SR	(Relay, Return)
2	P	TX+	(TTY Selector Drive)
3	T	GND	
4	S	SS	(+24v)
9	Q	TX-	(TTY Selector Drive)

7.8 J118 EIA (Mating Cable Connector Amphenol 17-20250-1)

PIN	TO*	SIGNAL
1	G	Ground
2	I	Data TX
3	F	Data RX
4	B	Request to Send
5	A	Clear To Send
6	C	Data Set Ready
7	H	Ground
8	D	Data Carrier Detect
11	K	Flag
18	L	$\overline{\text{FSO}}$
20	E	Data Terminal Ready
23	M	Rate
25	J	BUSY

7.9 J119 EIA (Mating Cable Connector Cinch DB 19604-432 mounted in a DB-51226-1 hood assembly or equivalent)
J119 has same wire connections as J118.

7.10 J120 CONTROL IN (Mating cable connector Amphenol 17-20150-1)
J121 CONTROL OUT (Mating cable connector Amphenol 17-10150-1)

PIN	TO*	SIGNAL	
1	E	M1	
2	C	M2	
3	B	M4	
4	P	M8	
J120-5	J	$\overline{\text{SPC}}$	(Print Out)
J121-5	L	$\overline{\text{SPCR}}$	(Print In)
6	I	$\overline{\text{ISD}}$	(Hold)
7	G	$\overline{\text{Daisy Stop}}$	
8	F	$\overline{\text{Daisy Start}}$	
9	H	$\overline{\text{Daisy Reset}}$	
10		Display 1	
11		Display 2	
12		Display 4	
13		Display 8	
14		Display Clock	
J121-15	K	Interlock	
J120-15	A	Ground	

NOTE: All like numbered pins are jumpered from J120 to J121 except pins 5, 15, and 10.

7.11 J122 PRINTER (Mating Cable Plug Amphenol 17-20500-1)

PIN	SIGNAL	PIN	SIGNAL
1	Data 1	26	Data 4
2	Data 2	27	Data 8
3	Data 10	28	Data 40
4	Data 20	29	Data 80
5	Data 100	30	Data 400
6	Data 200	31	Data 800
7	Data 1K	32	Data 4K
8	Data 2K	33	Data 8K
9	Data 10K	34	Data 40K
10	Data 20K	35	Data 80K
11	Data 100K	36	Data 400K
12	Data 200K	37	Data 800K
13	Address 1	38	Address 4
14	Address 2	39	Address 8
15	Address 10	40	Address 40
16	Address 20	41	Address 80
17	Address 100	42	Address 400
18	Address 200	43	Address 800
19	Address 1K	44	Address 4K
20	Address 2K	45	Address 8K
21	+ Gate	46	Ground
22	No Connection	47	No Connection
23	+ Print Command	48	-PC
24	-Ref	49	$\overline{PBSY}$
25	+Ref	50	Ground